



#1961
3-7-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : **Confirmation No. 2601**
Mitsuaki OSHIMA et al. : **Docket No. 2000_1326**
Serial No. 09/669,916 : **Group Art Unit 2634**
Filed September 25, 2000 : **Examiner A. Le**
COMMUNICATION SYSTEM :

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ACCOUNT NO. 23-0975

Sir:

As required by the Examiner in the Office Action mailed August 28, 2002, 178 sheets of
formal (8½ x 11) drawings (Figs. 1-179) are submitted herewith.

Respectfully submitted,

Mitsuaki OSHIMA et al.

By: 

Jeffrey R. Filipak
Registration No. 41,471
Attorney for Patentees

JRF/fs
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
February 28, 2003

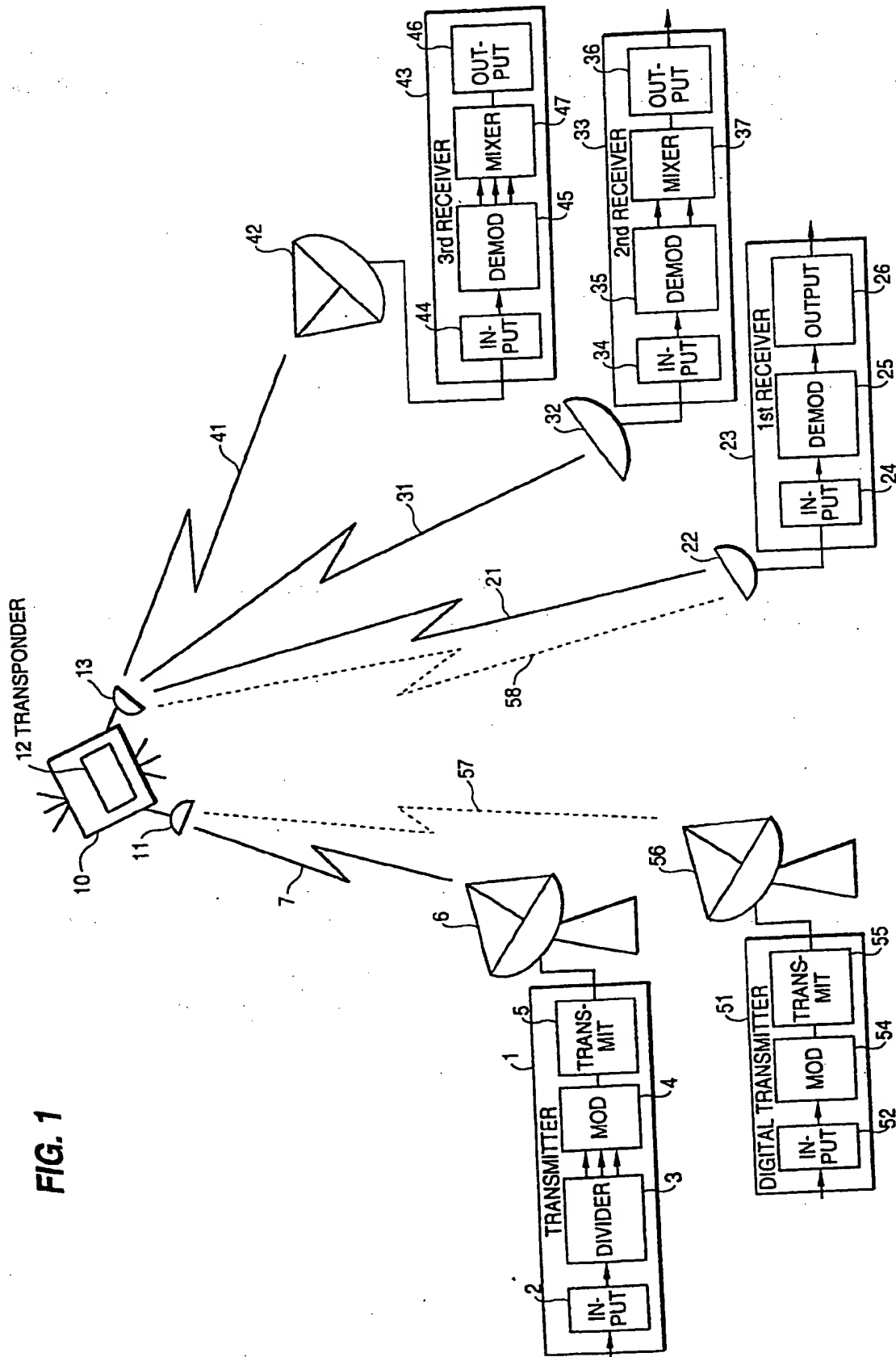


FIG. 2

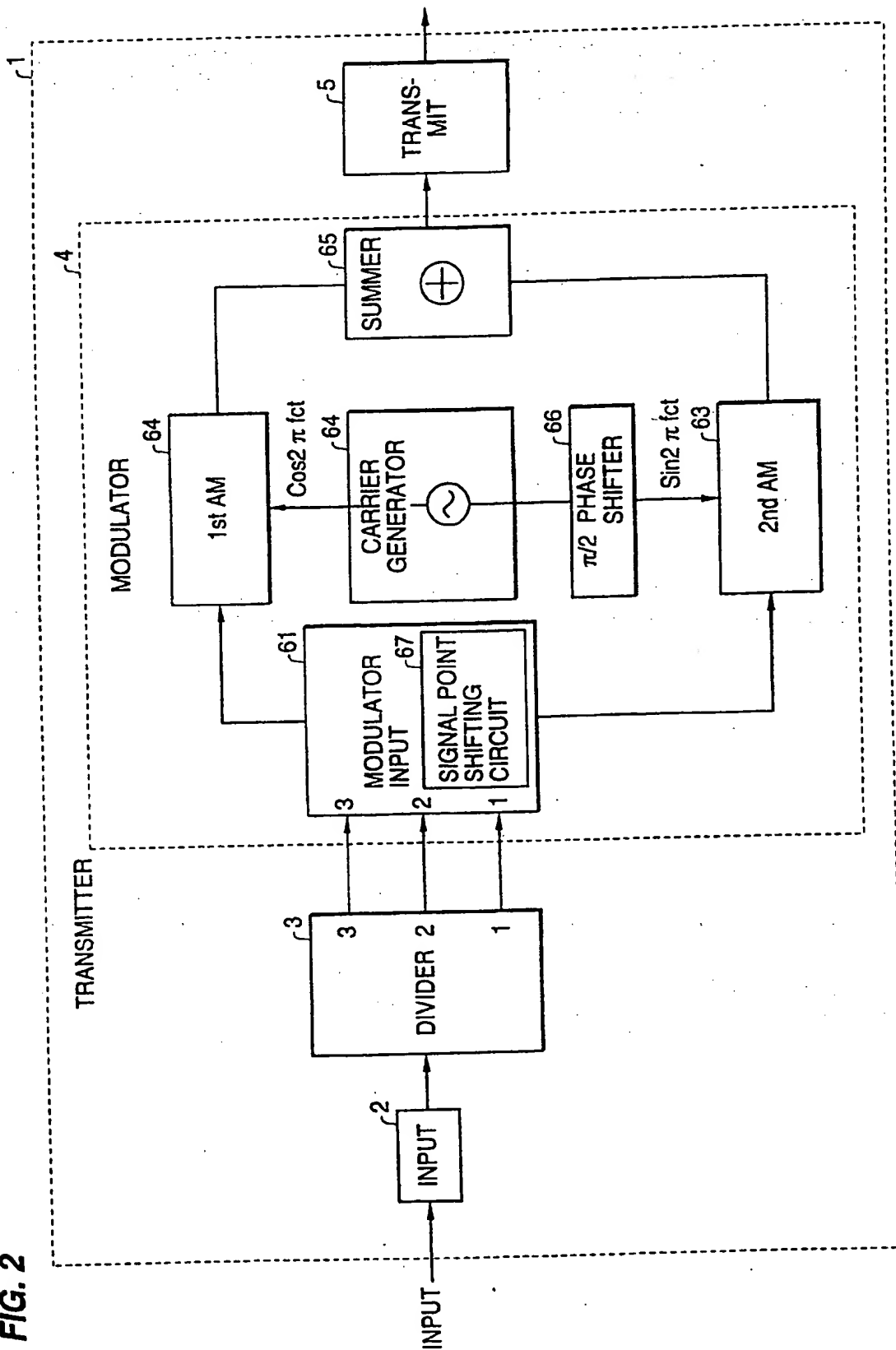


FIG. 3

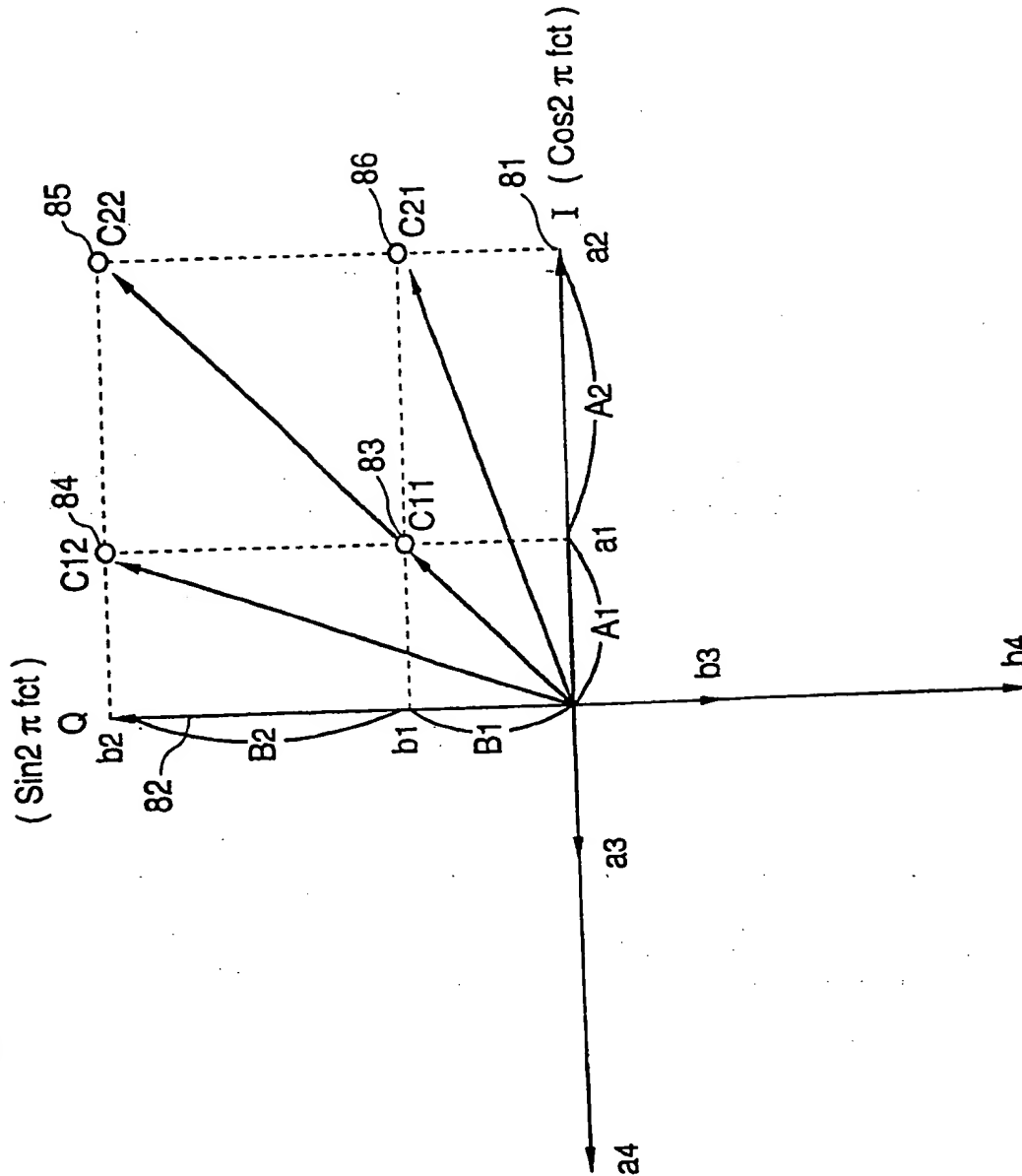


FIG. 4

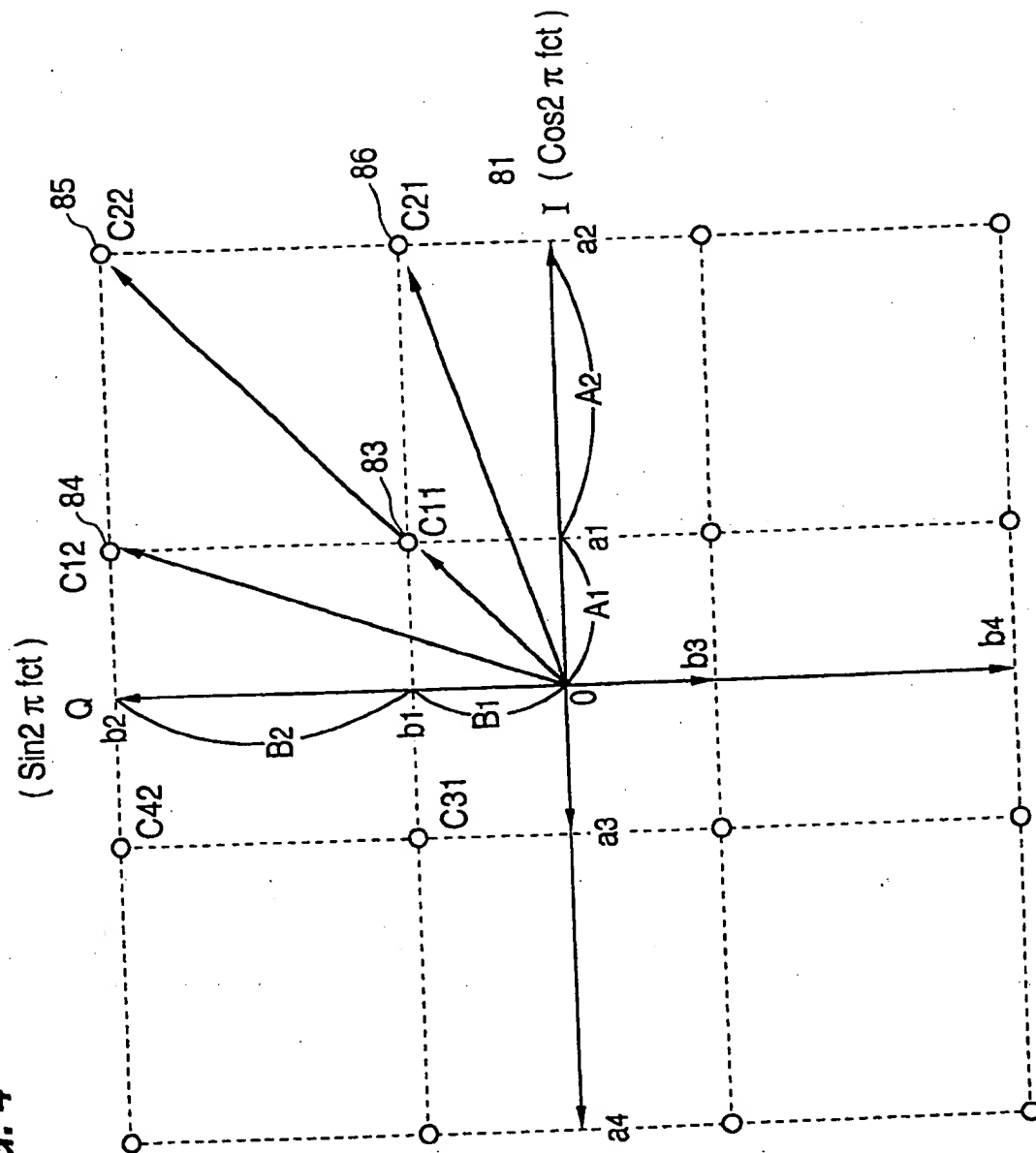


FIG. 5

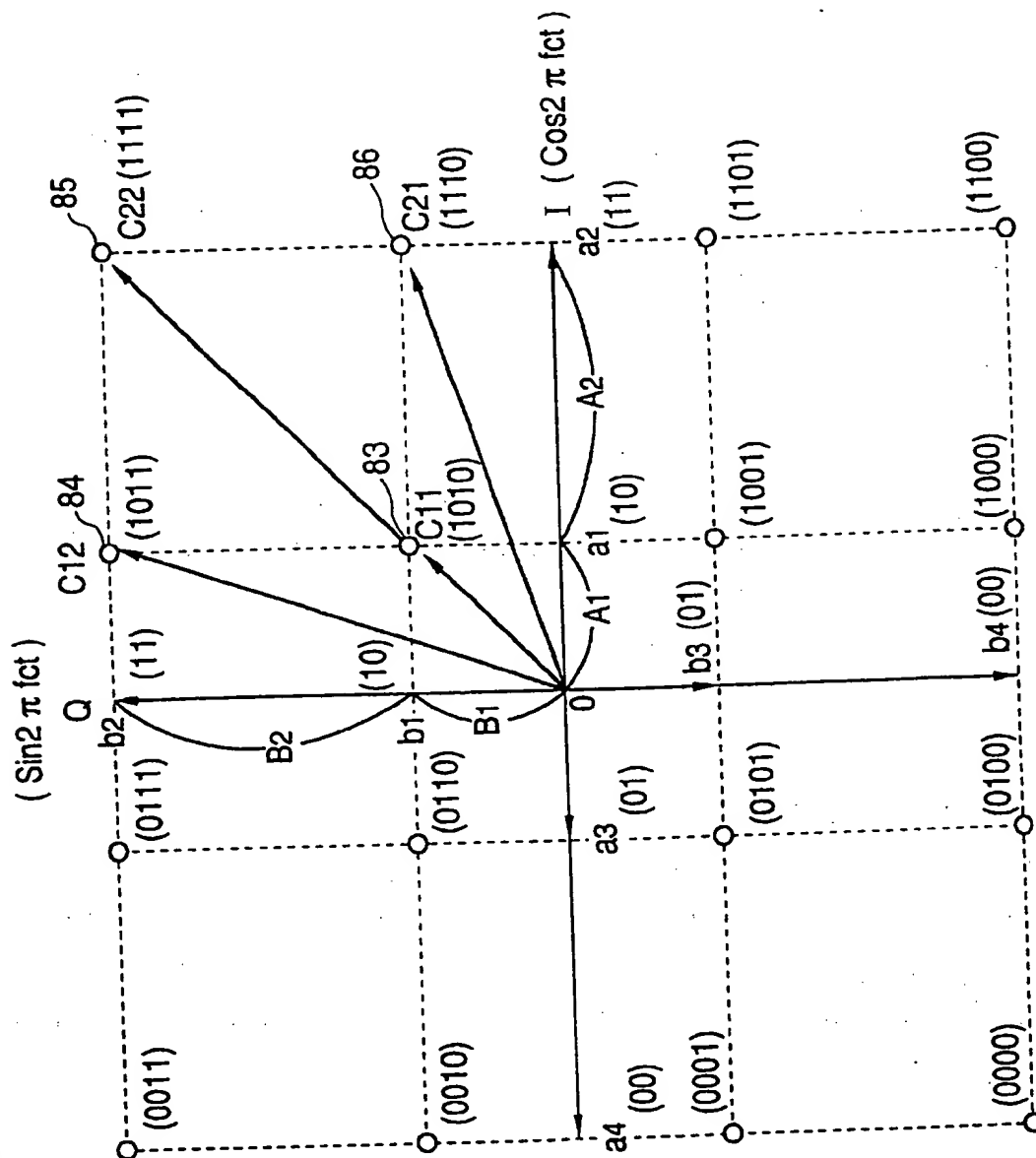


FIG. 6

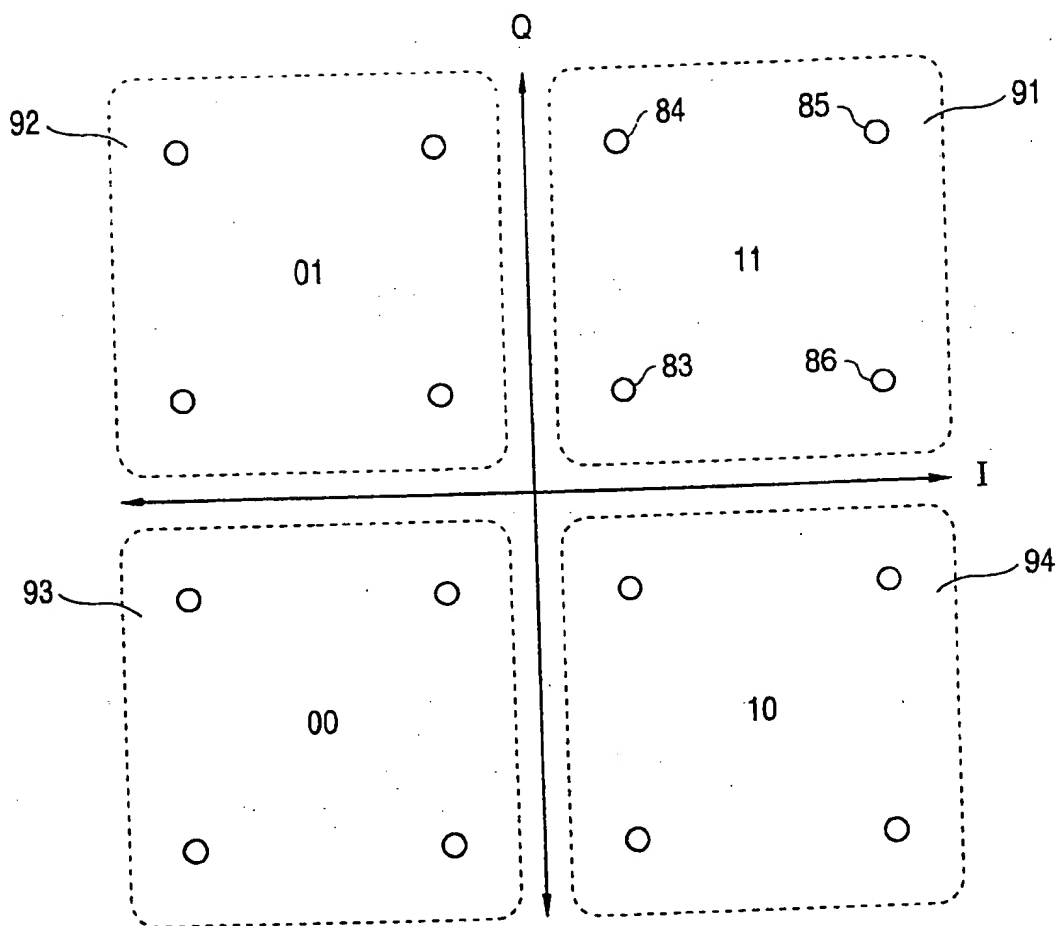


FIG. 7

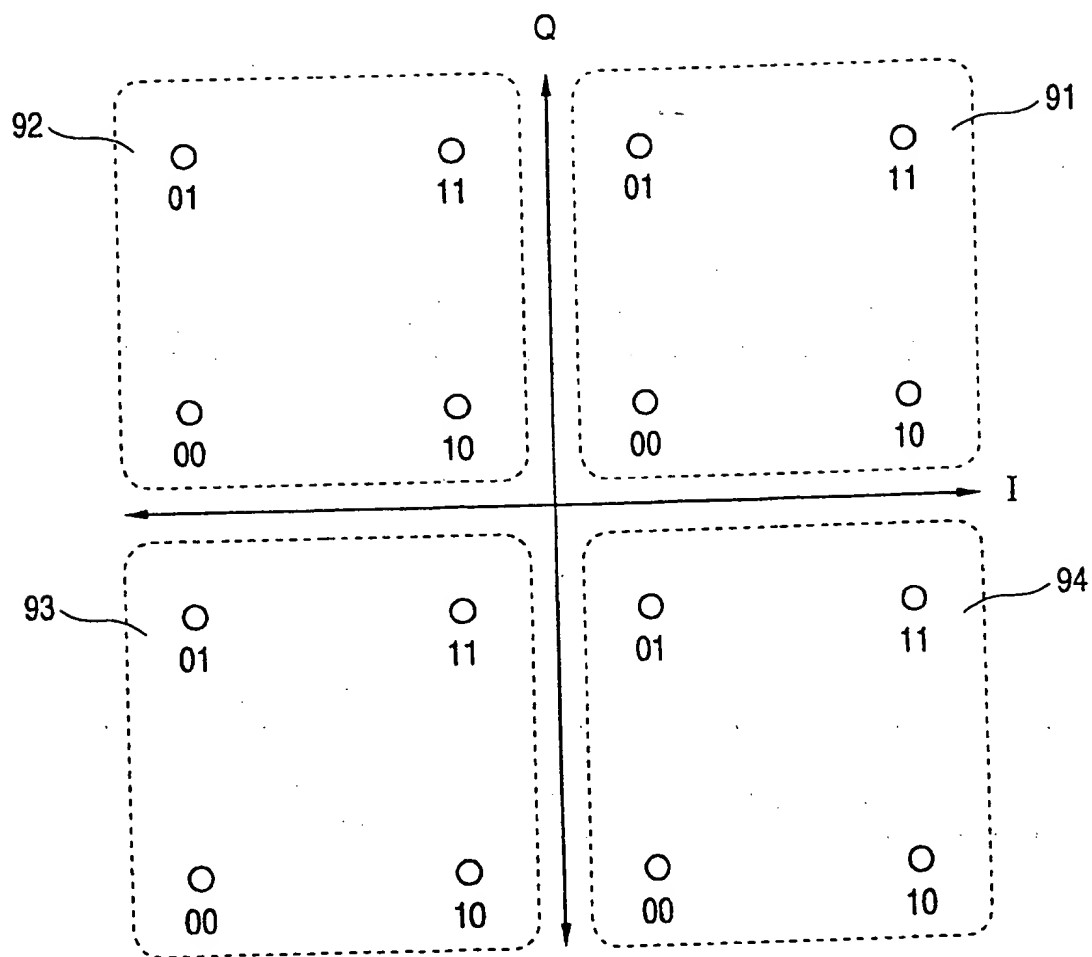


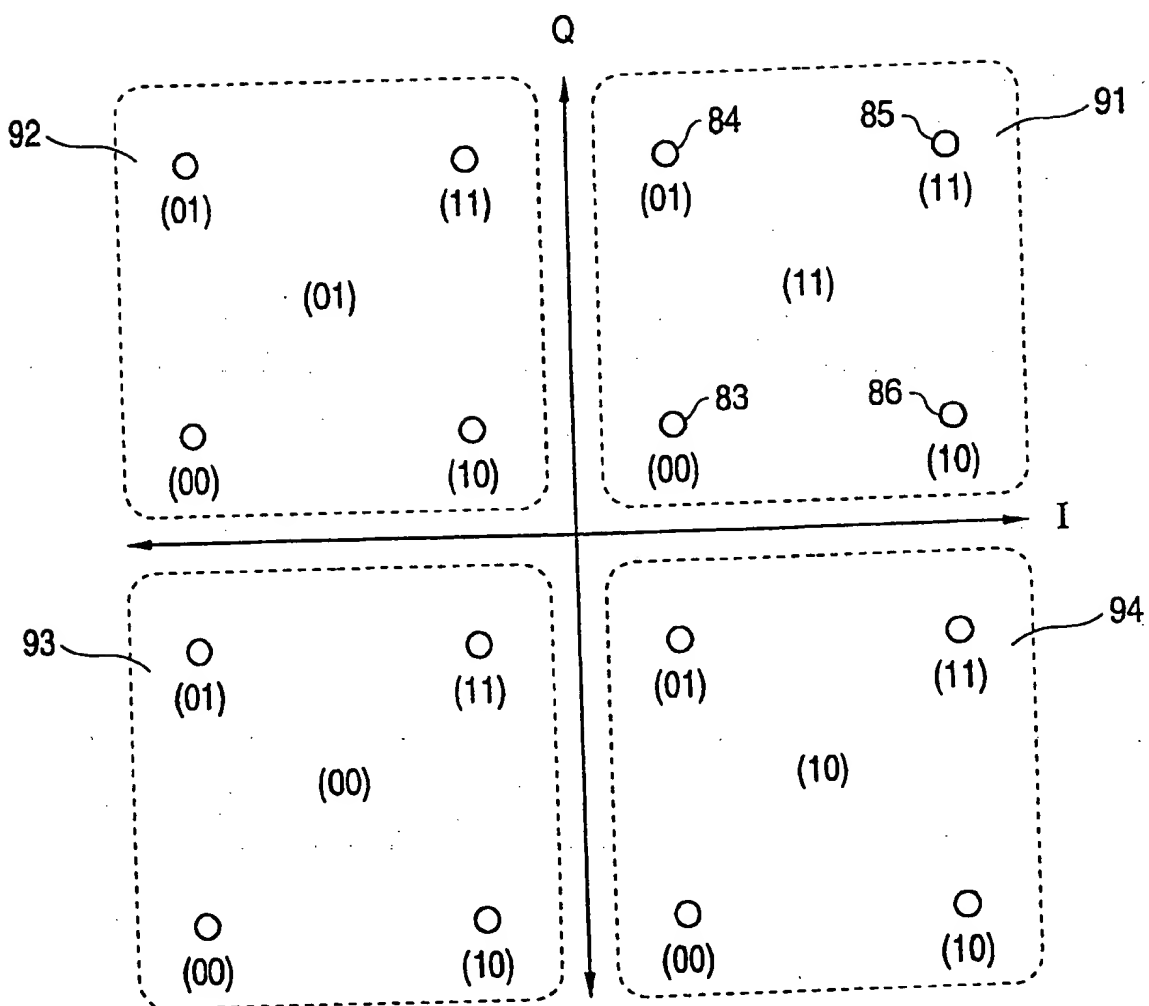
FIG. 8

FIG. 9

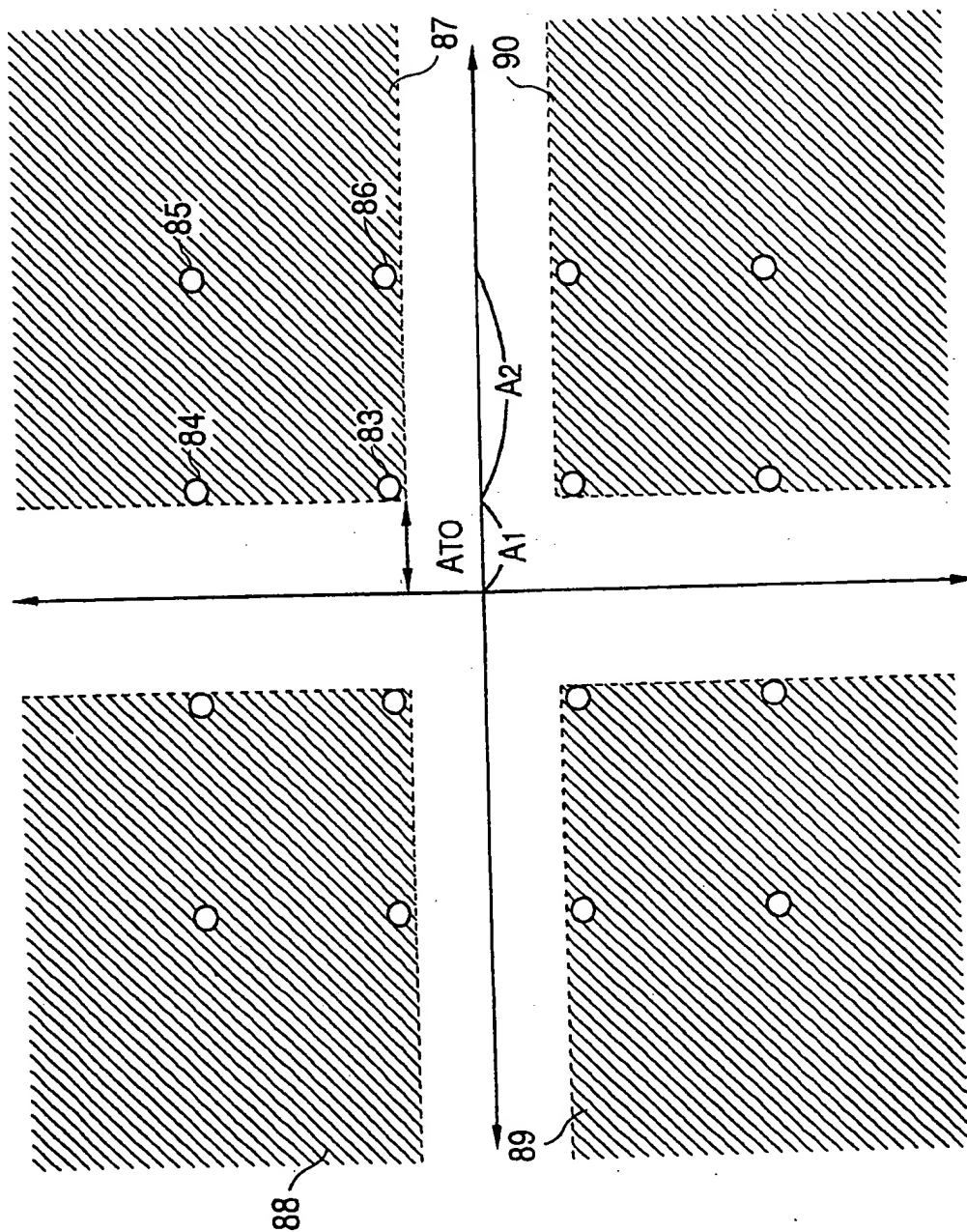


FIG. 10

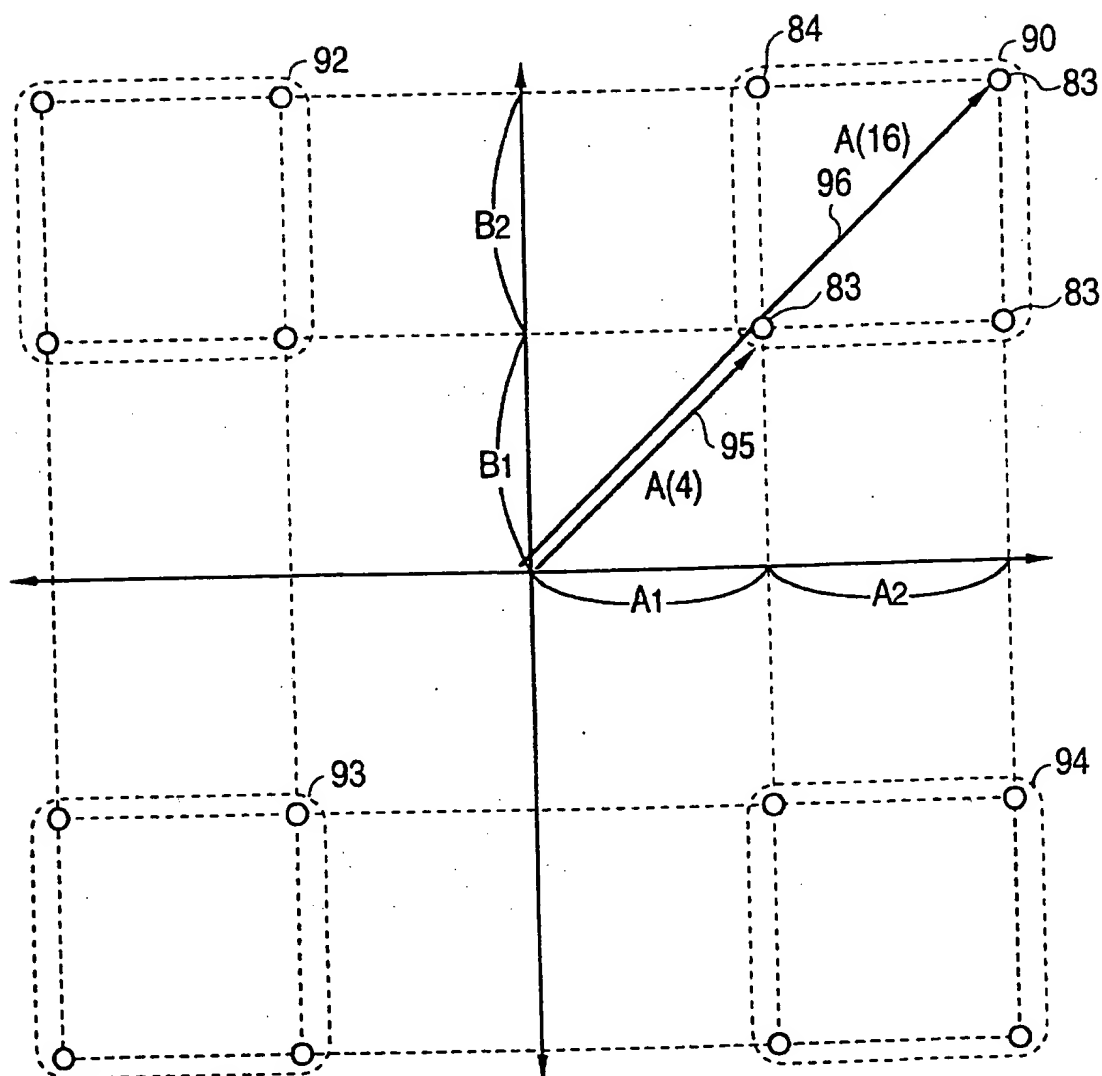


FIG. 11

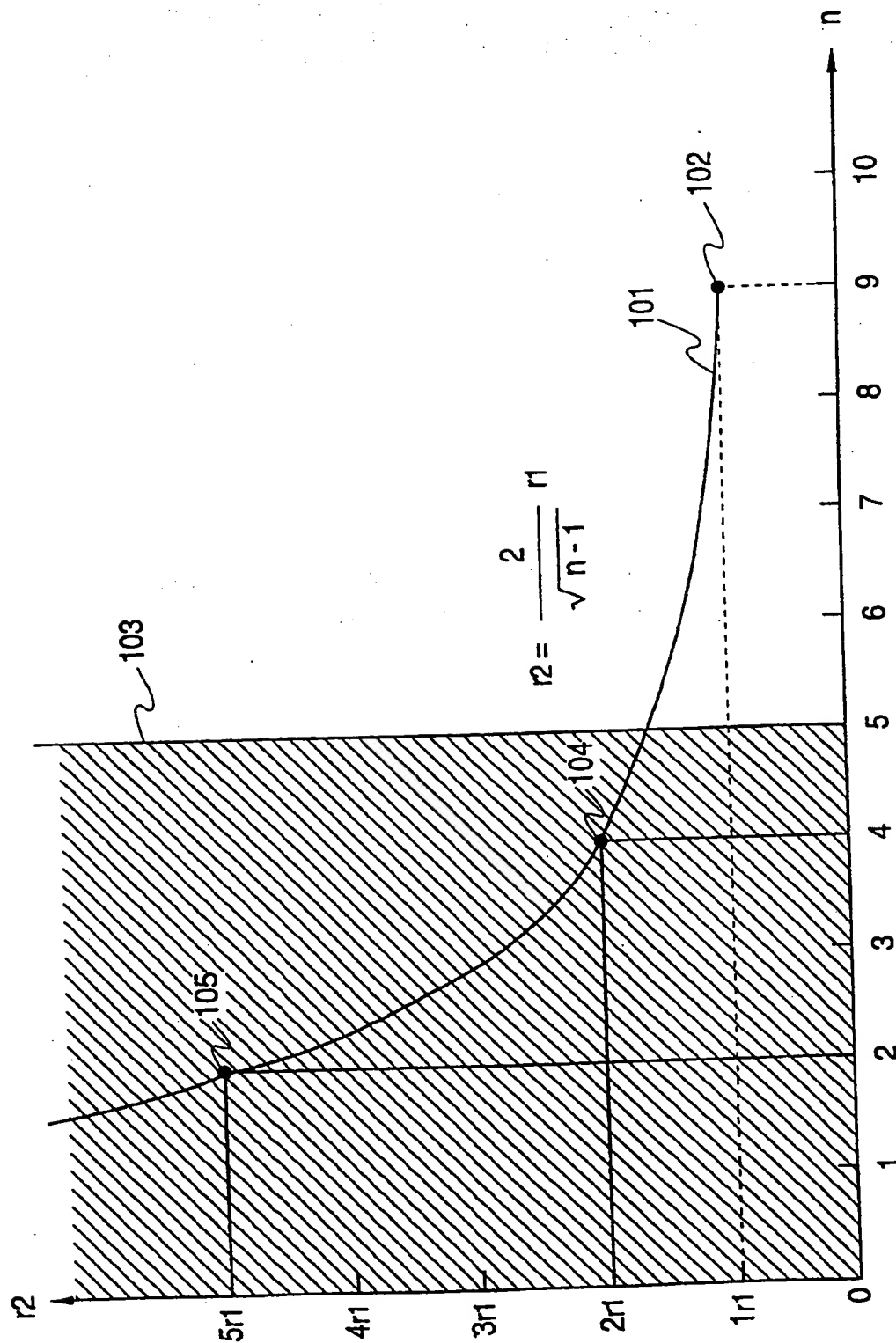


FIG. 12

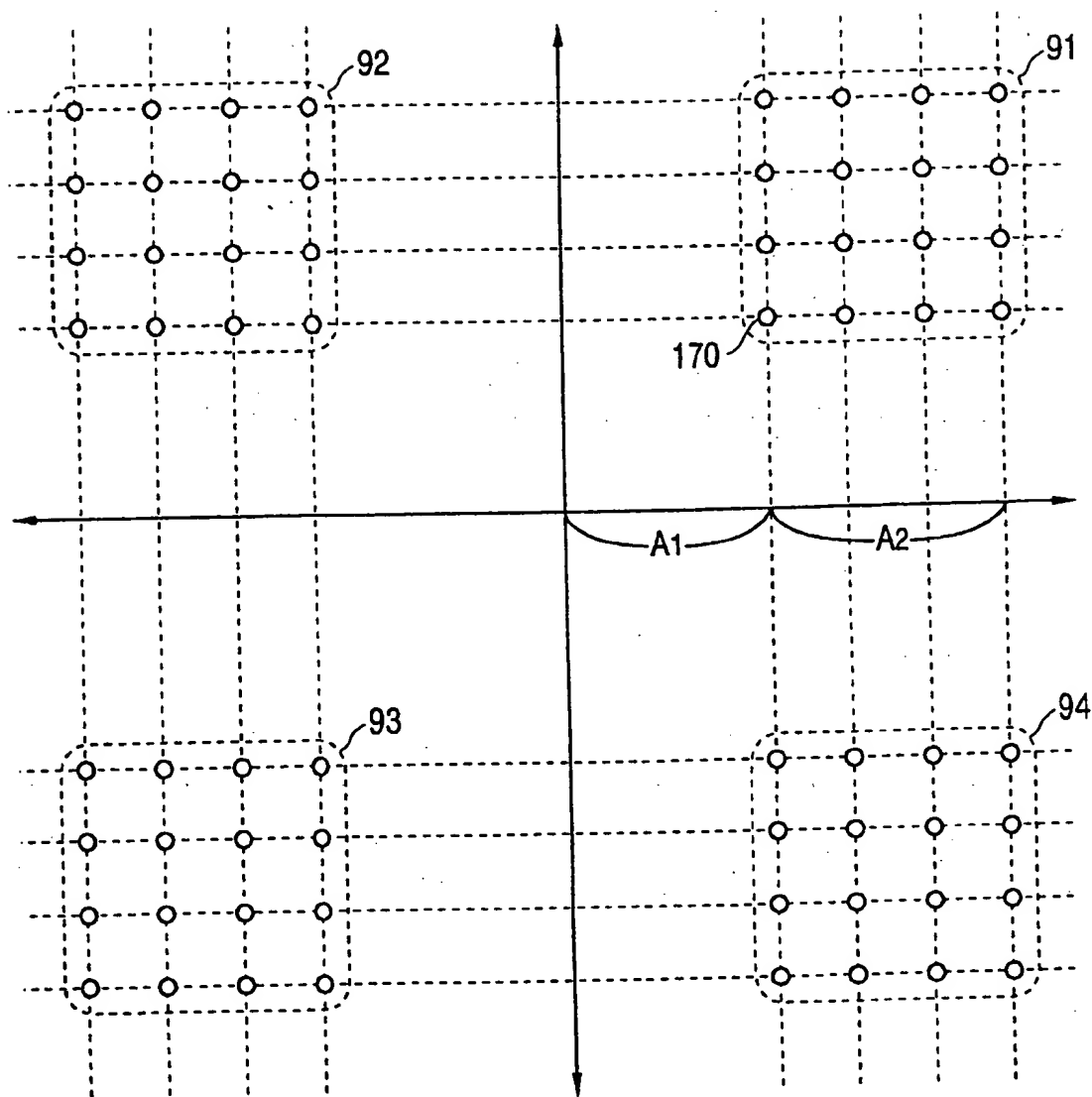


FIG. 13

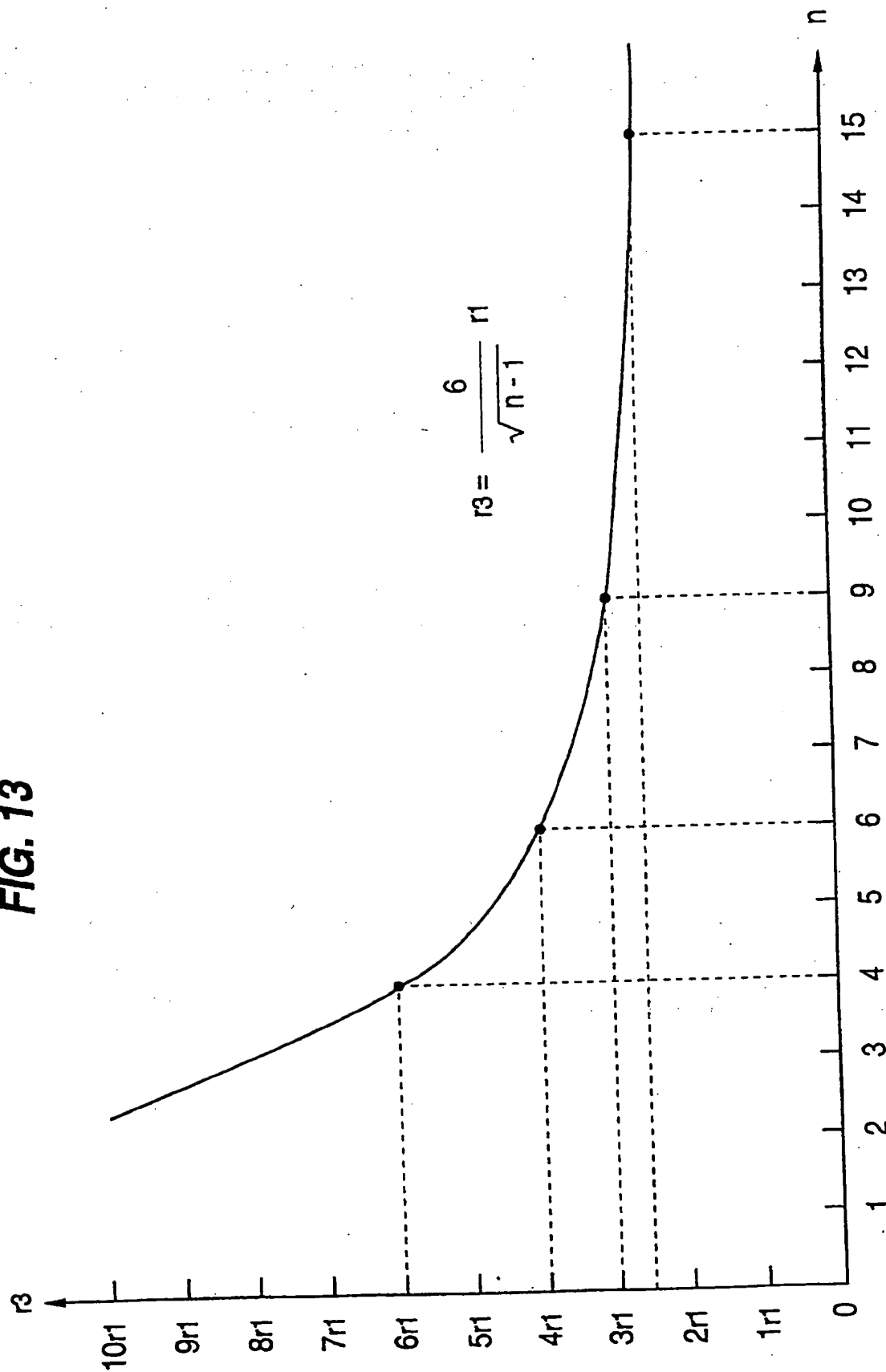


FIG. 14

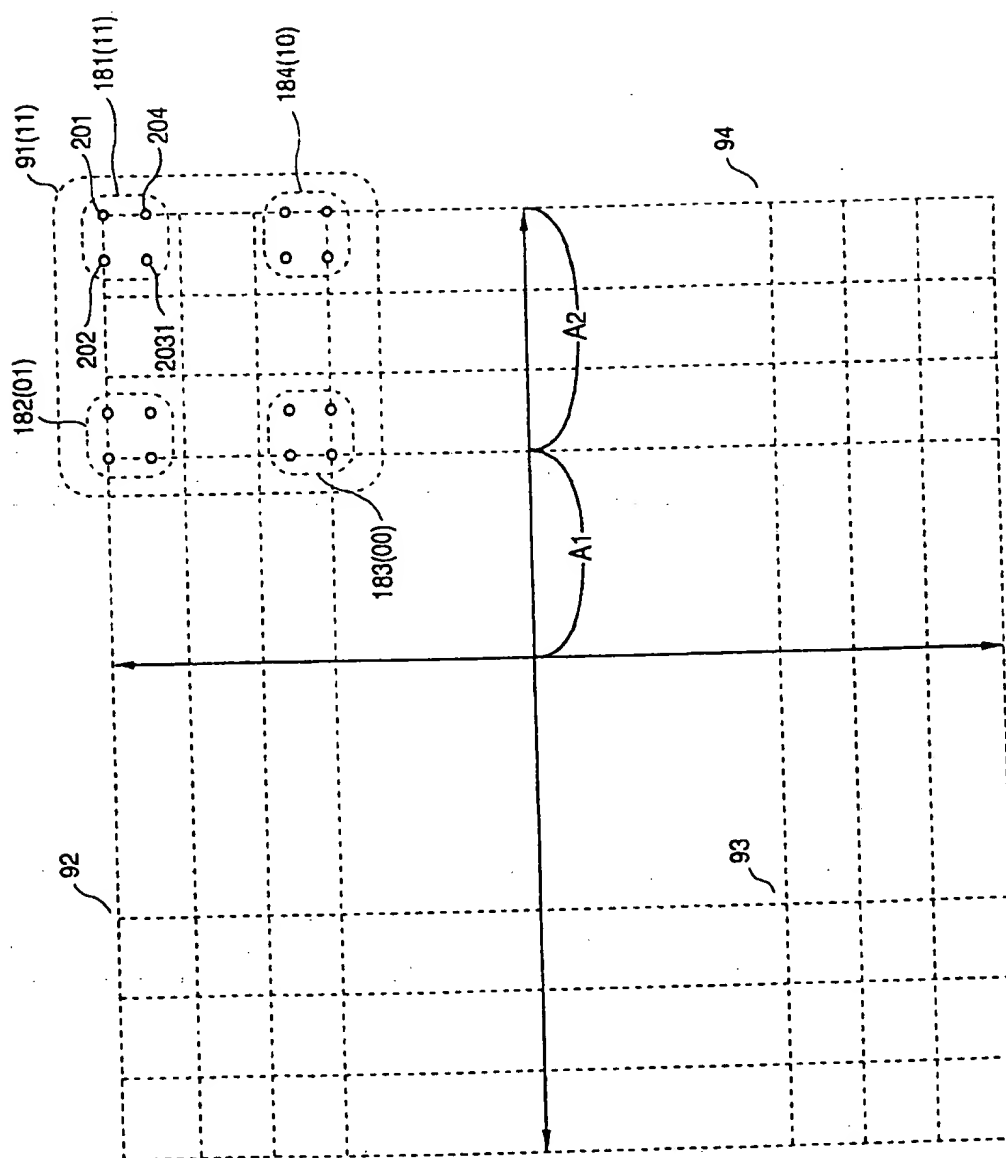


FIG. 15

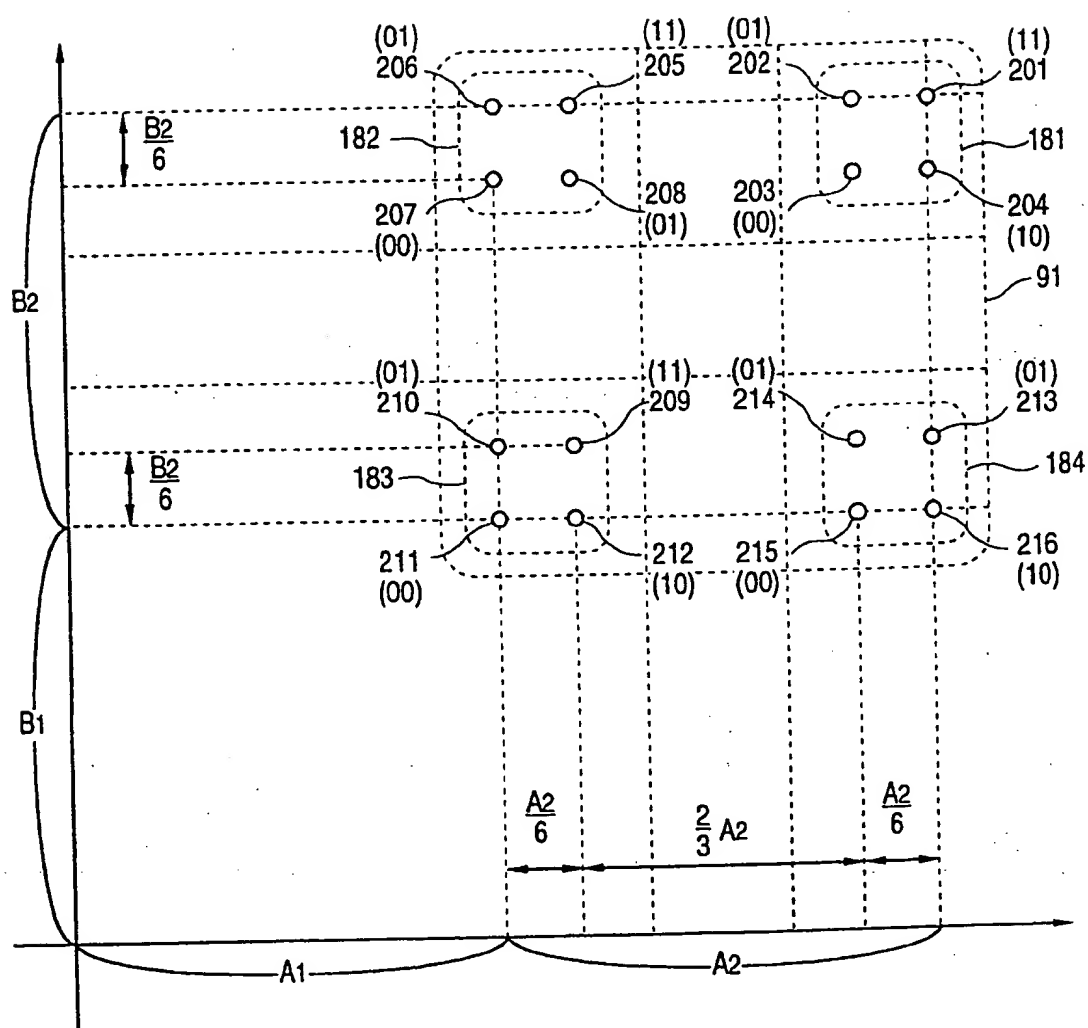


FIG. 16

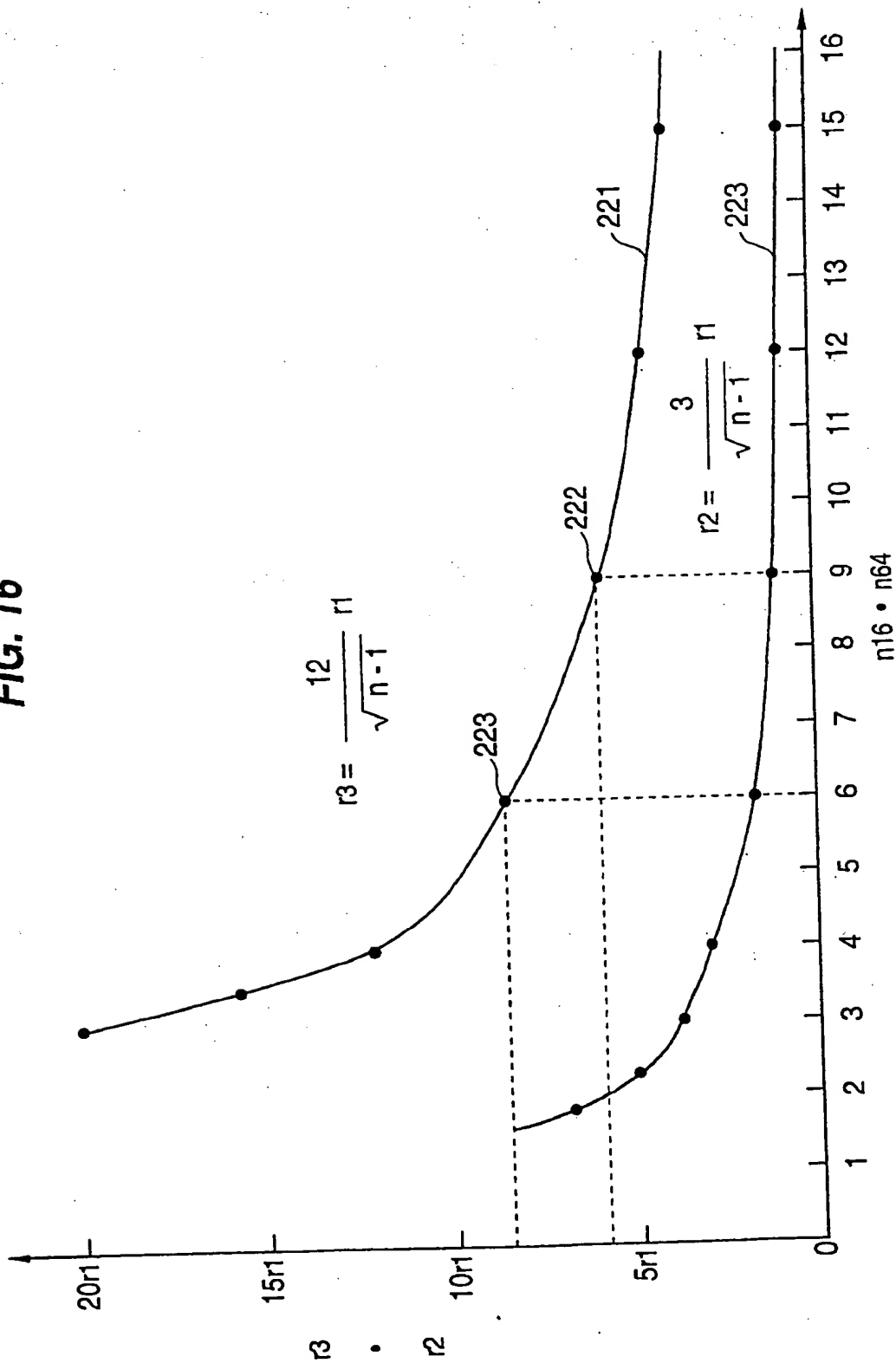


FIG. 17

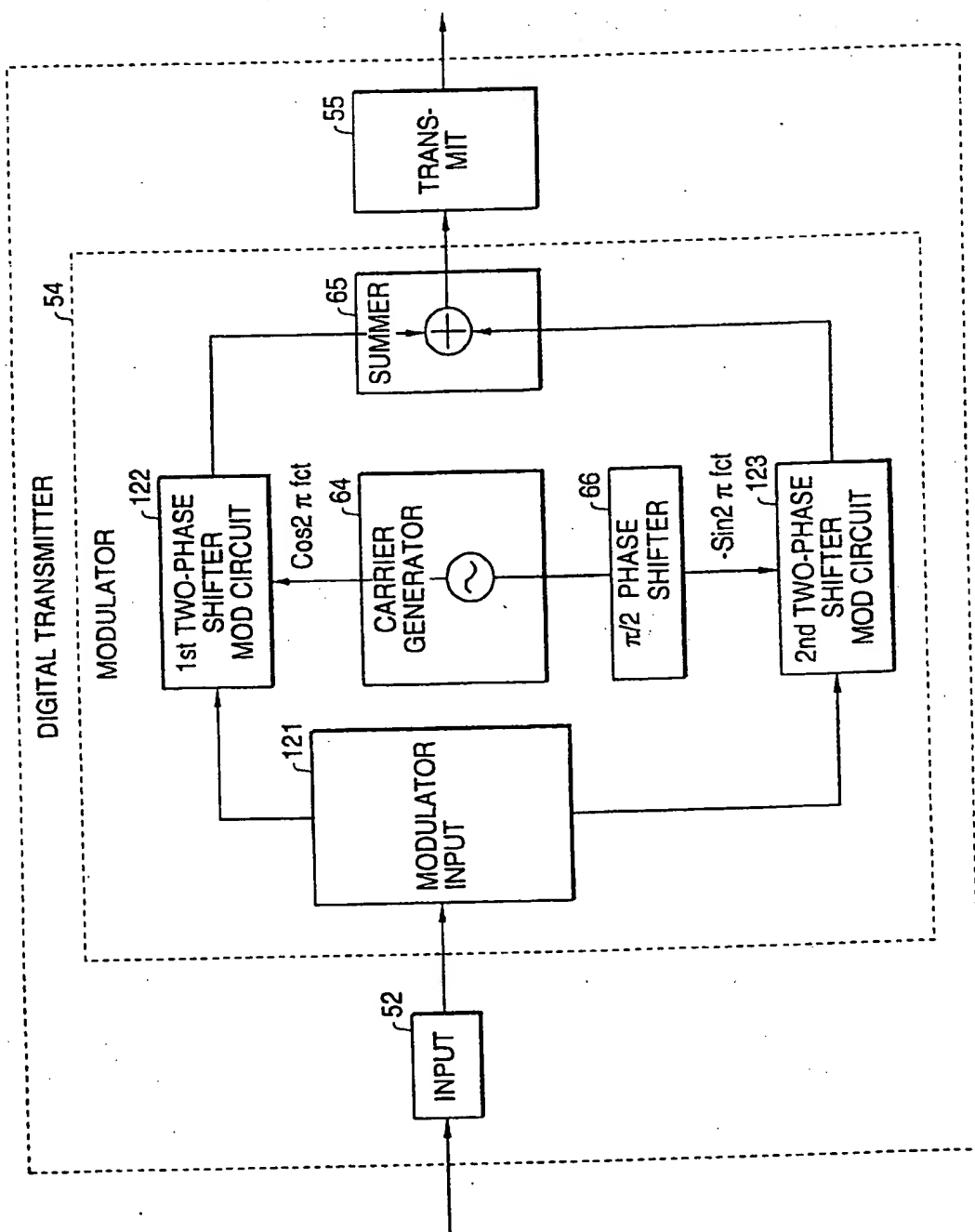


FIG. 18

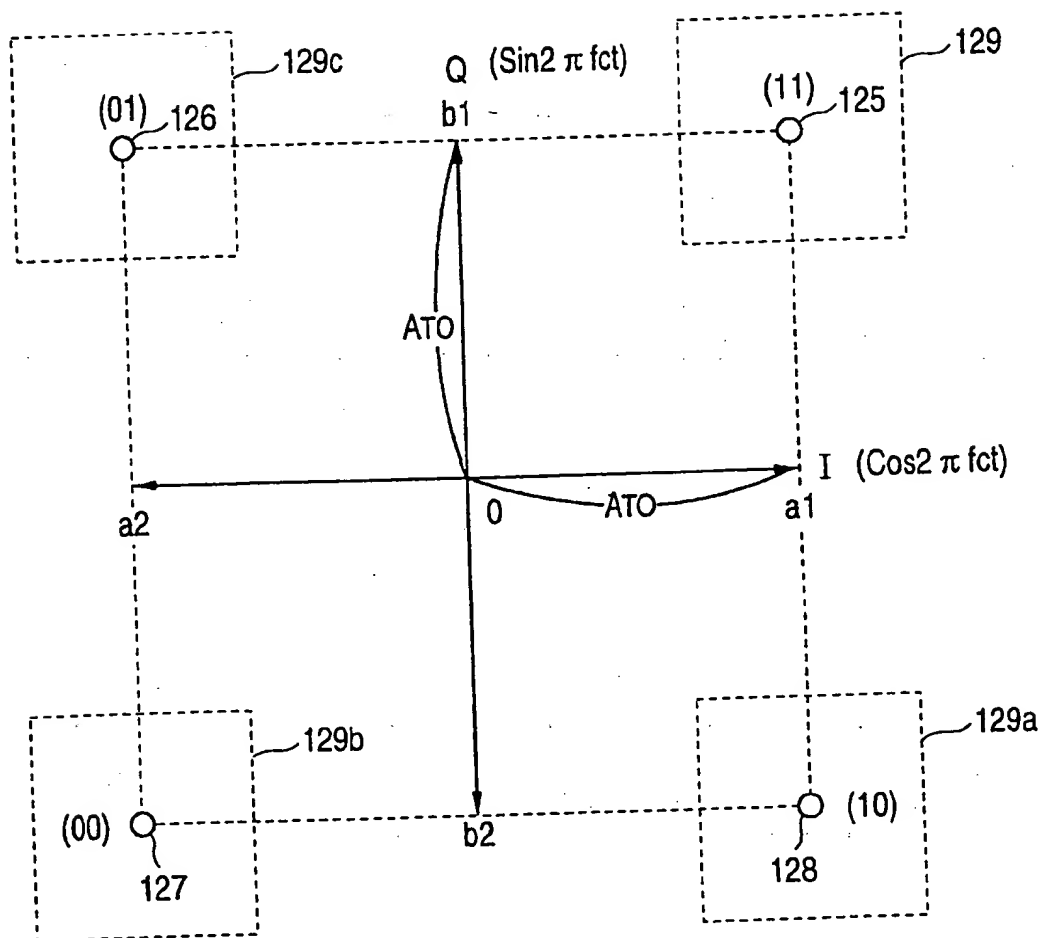


FIG. 19

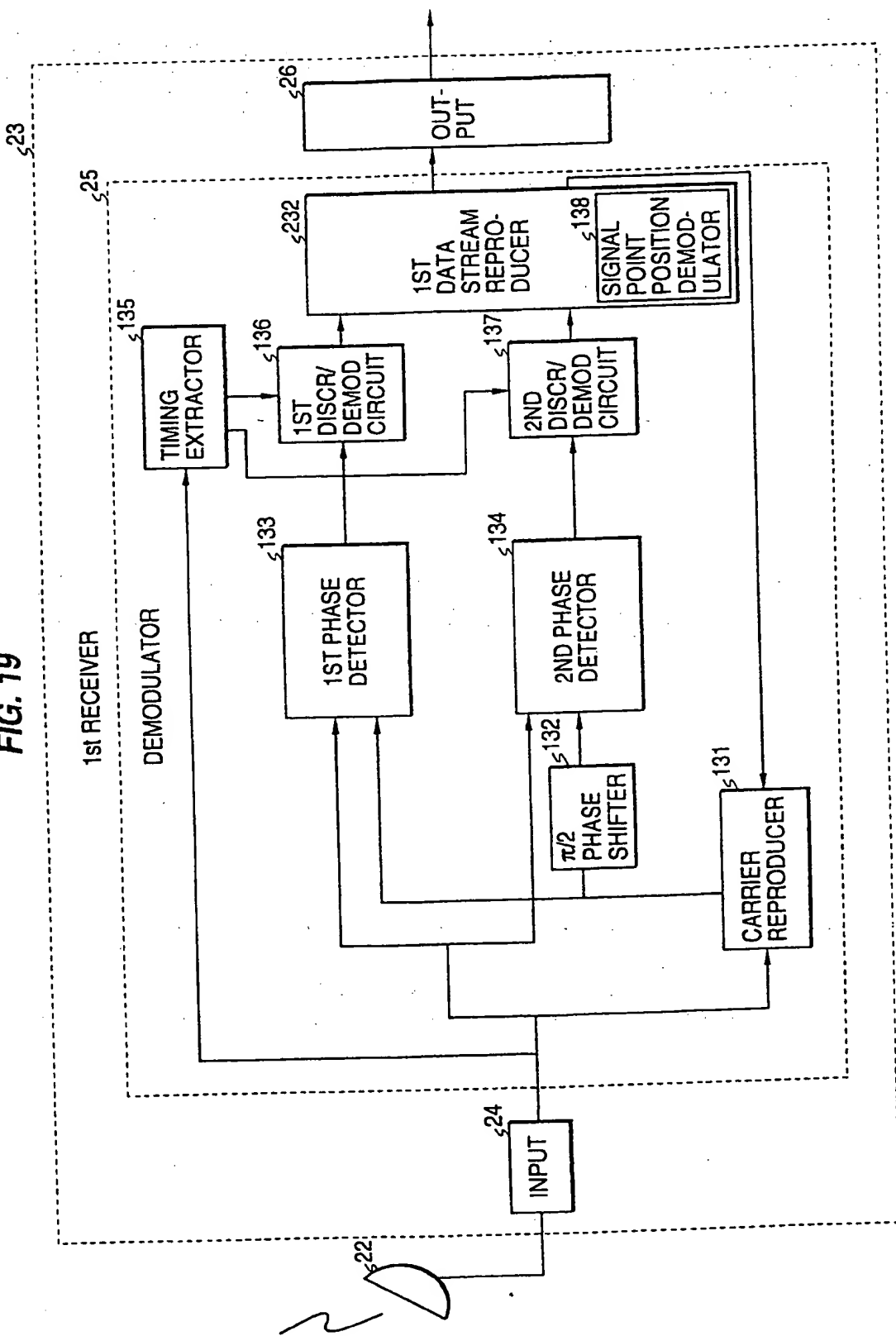


FIG. 20

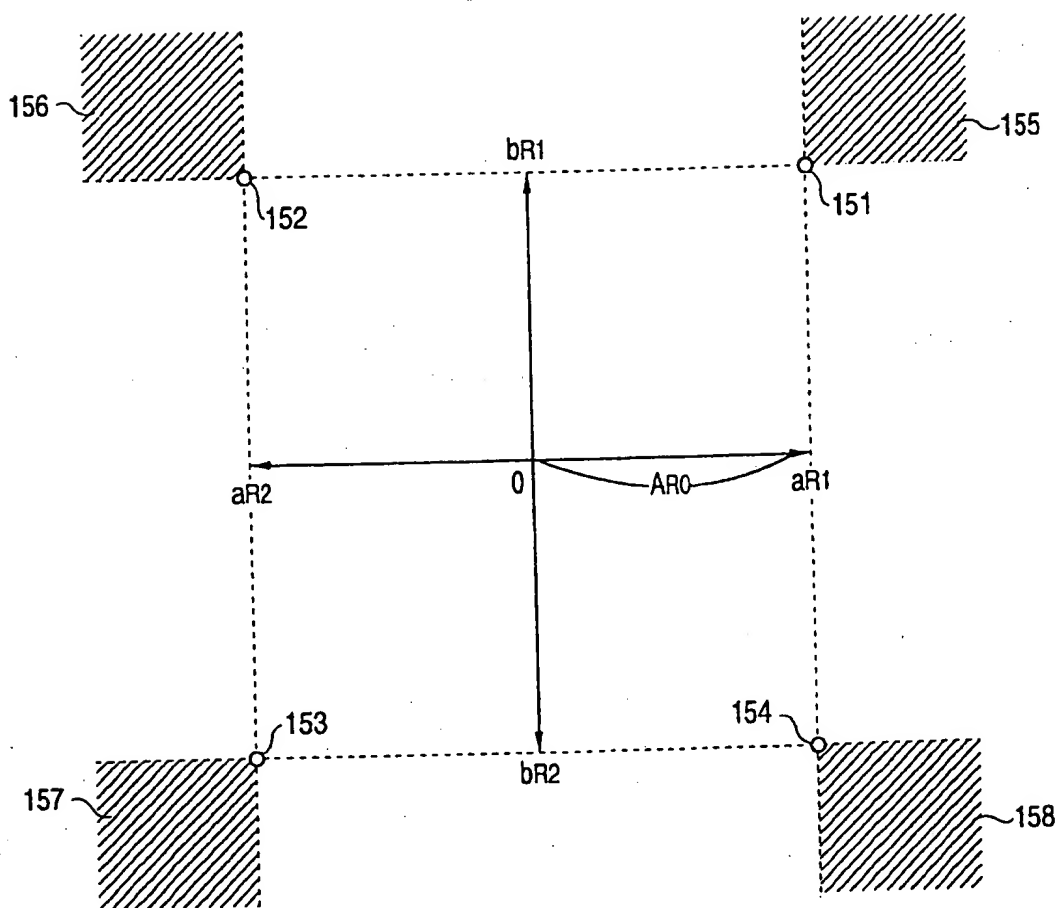


FIG. 21

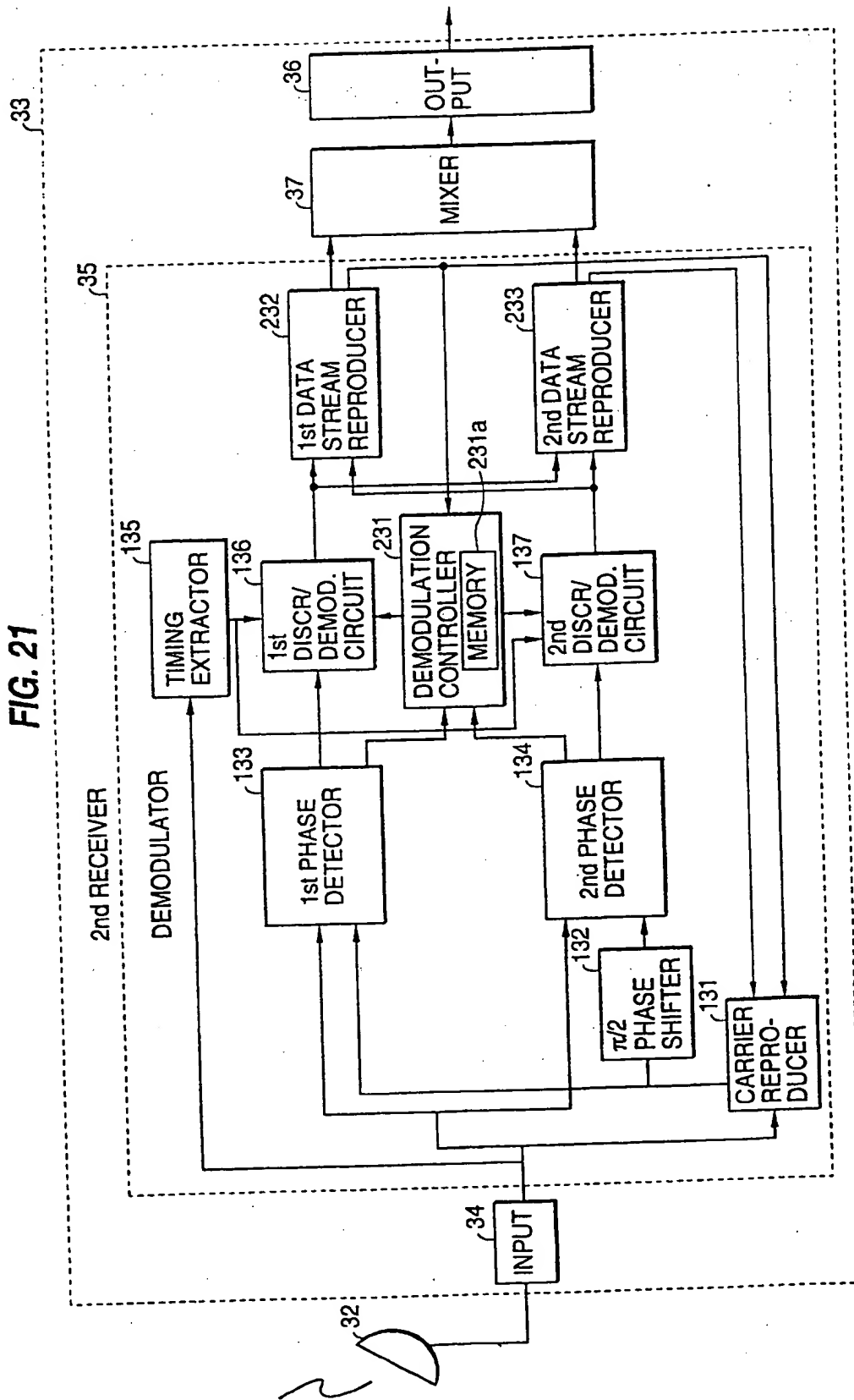


FIG. 22

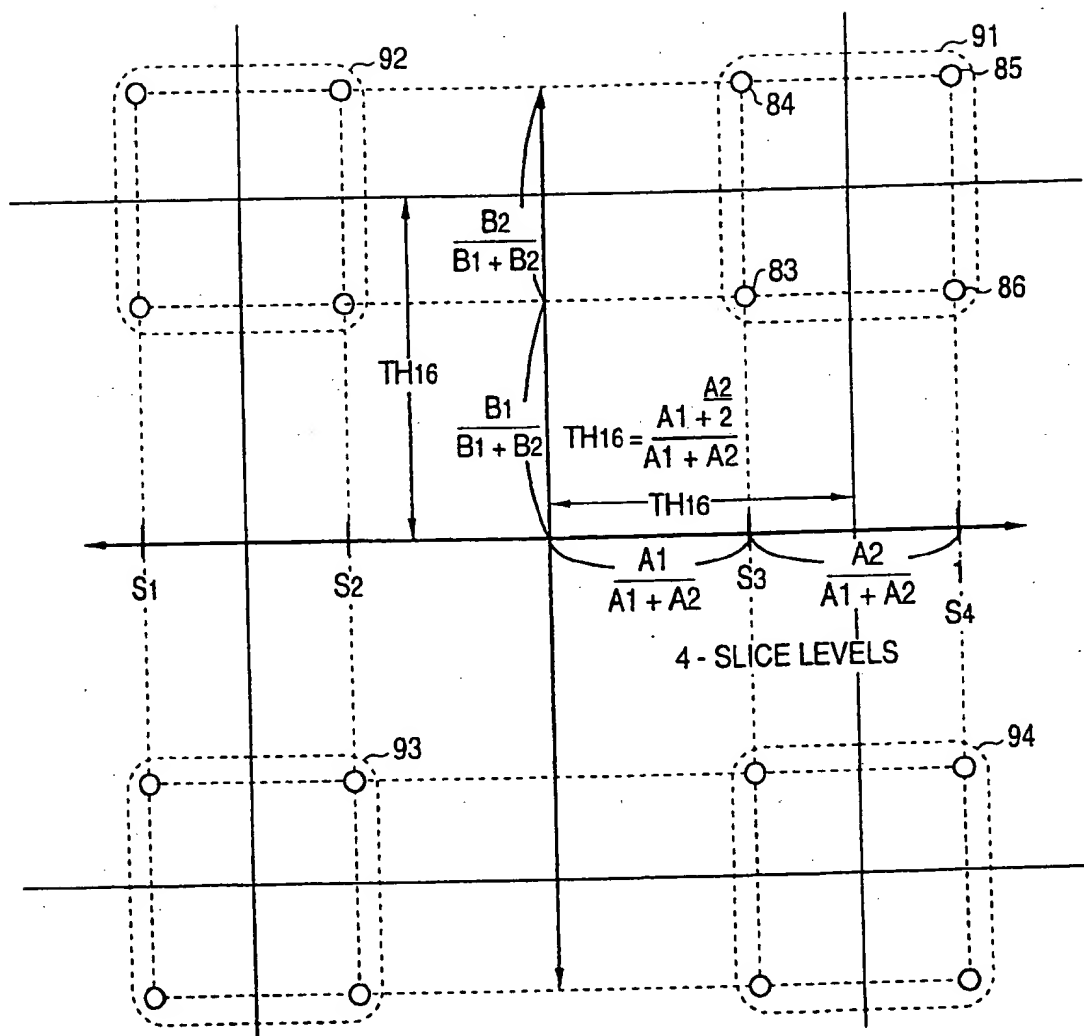


FIG. 24

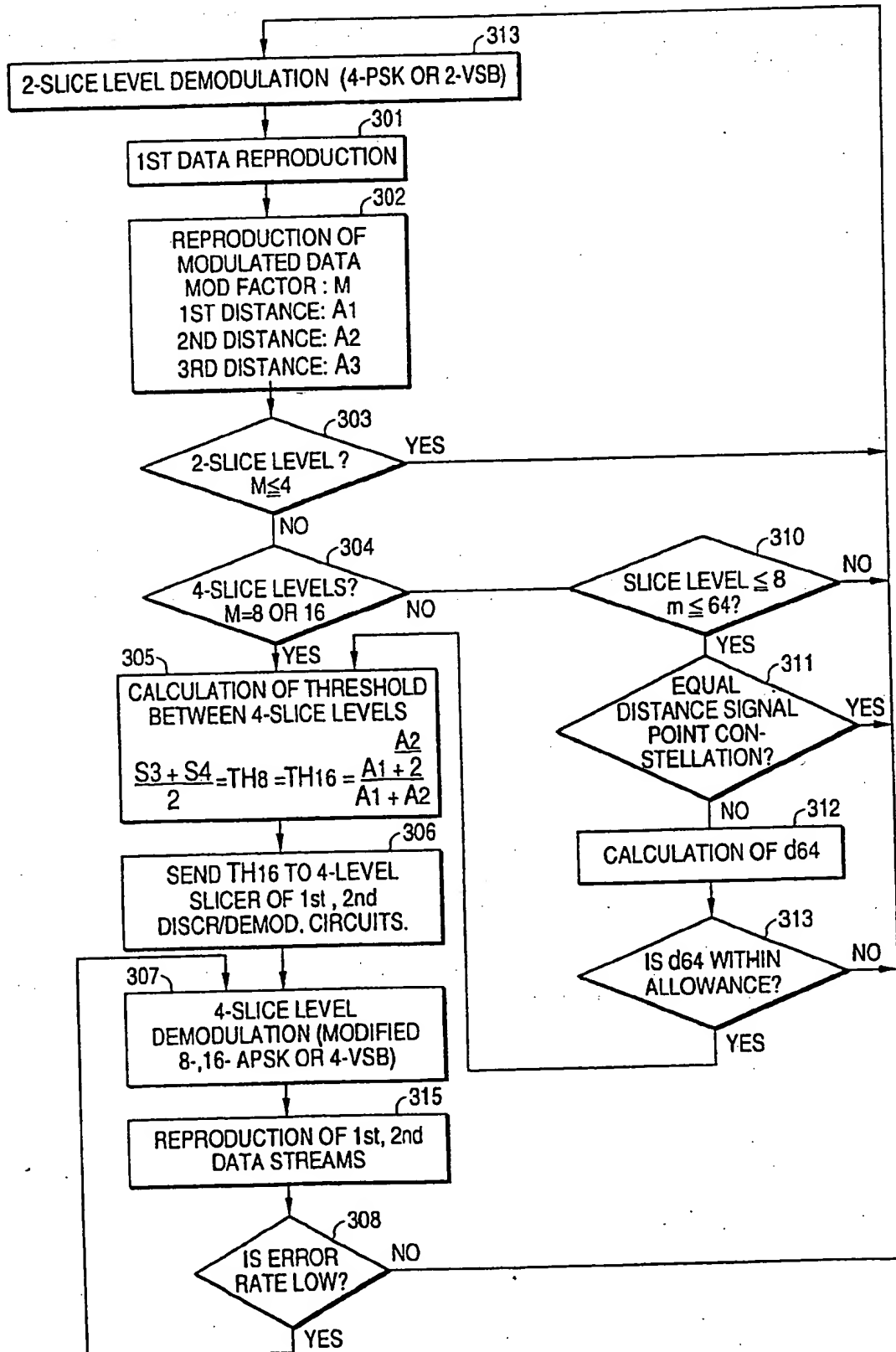


FIG. 25(a)

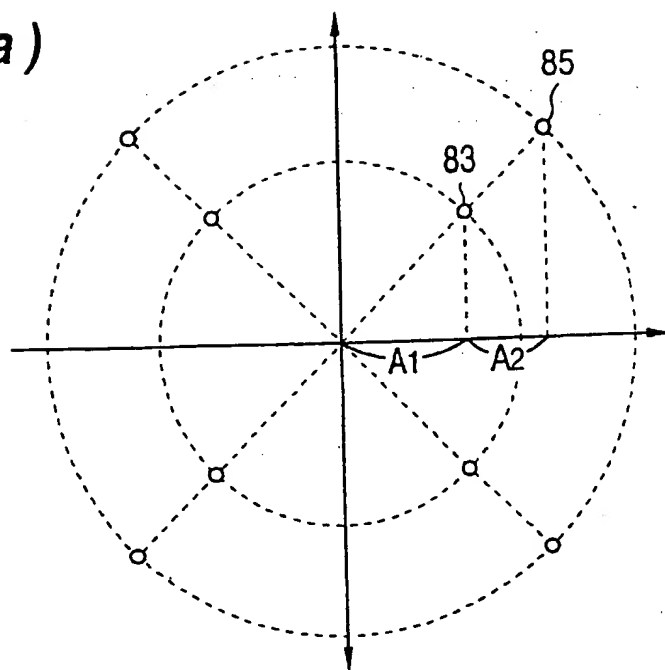


FIG. 25(b)

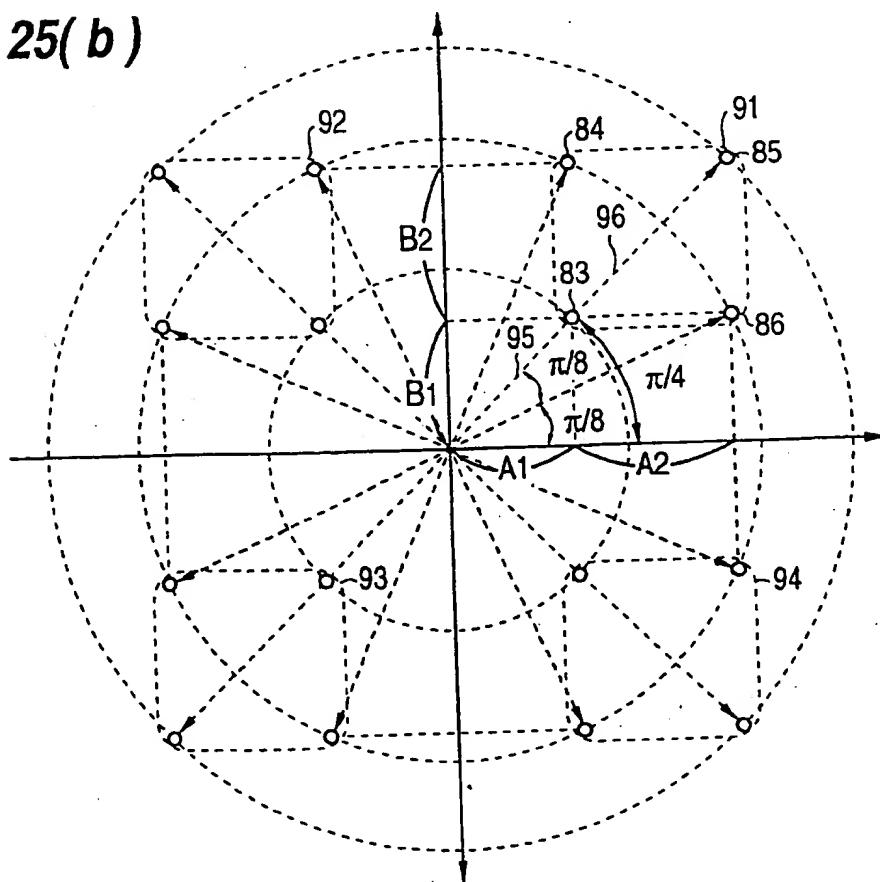
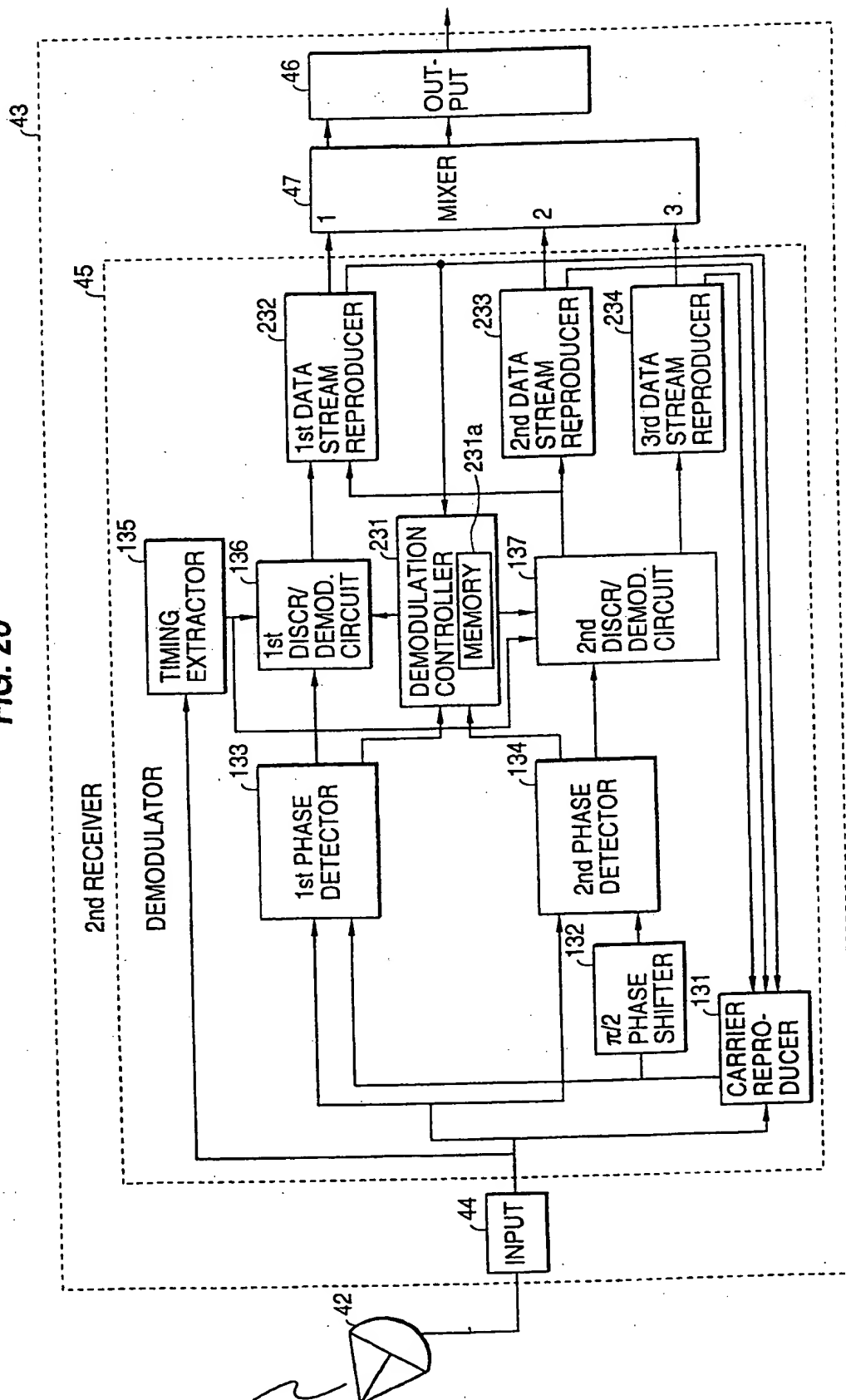


FIG. 26



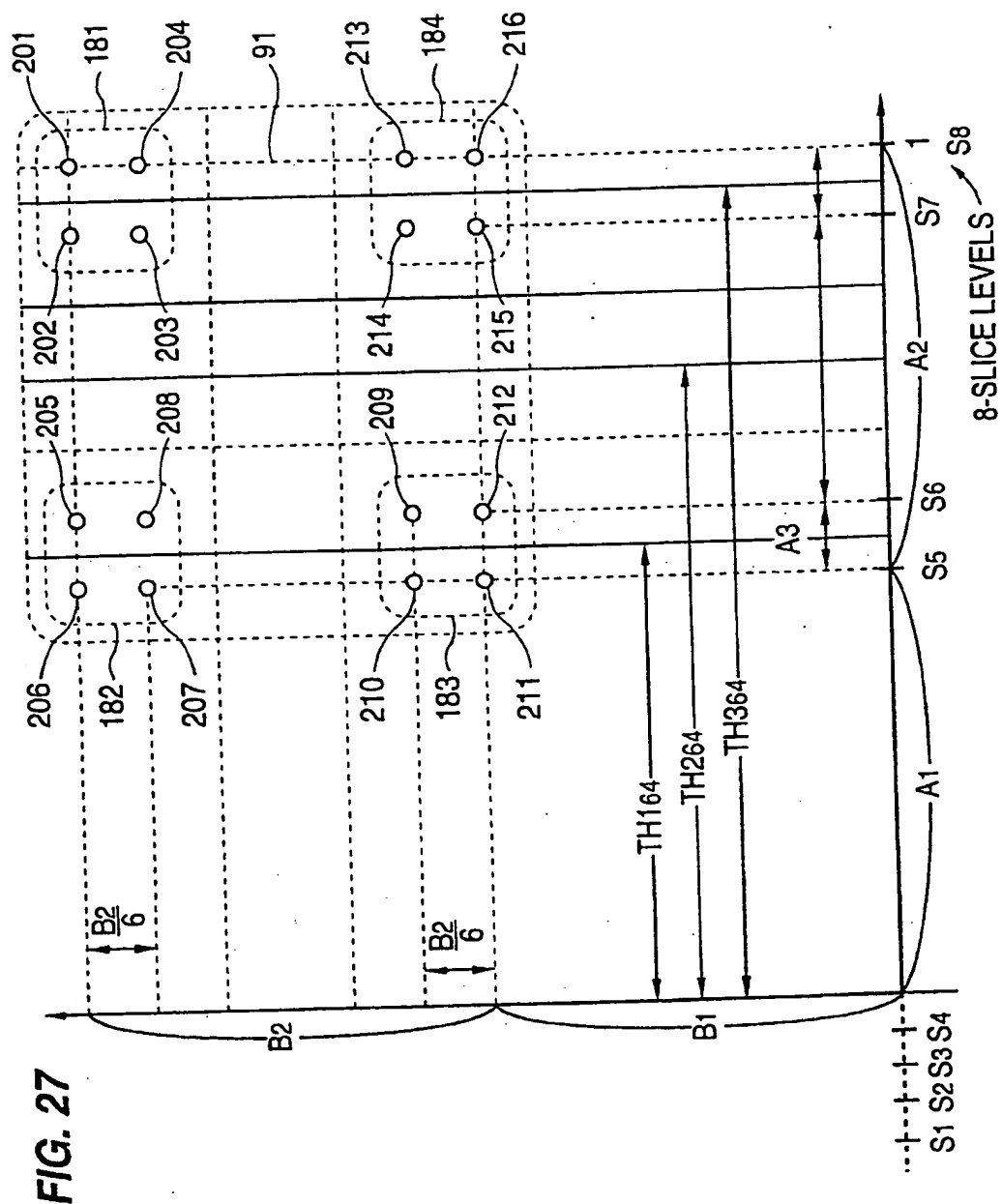


FIG. 28

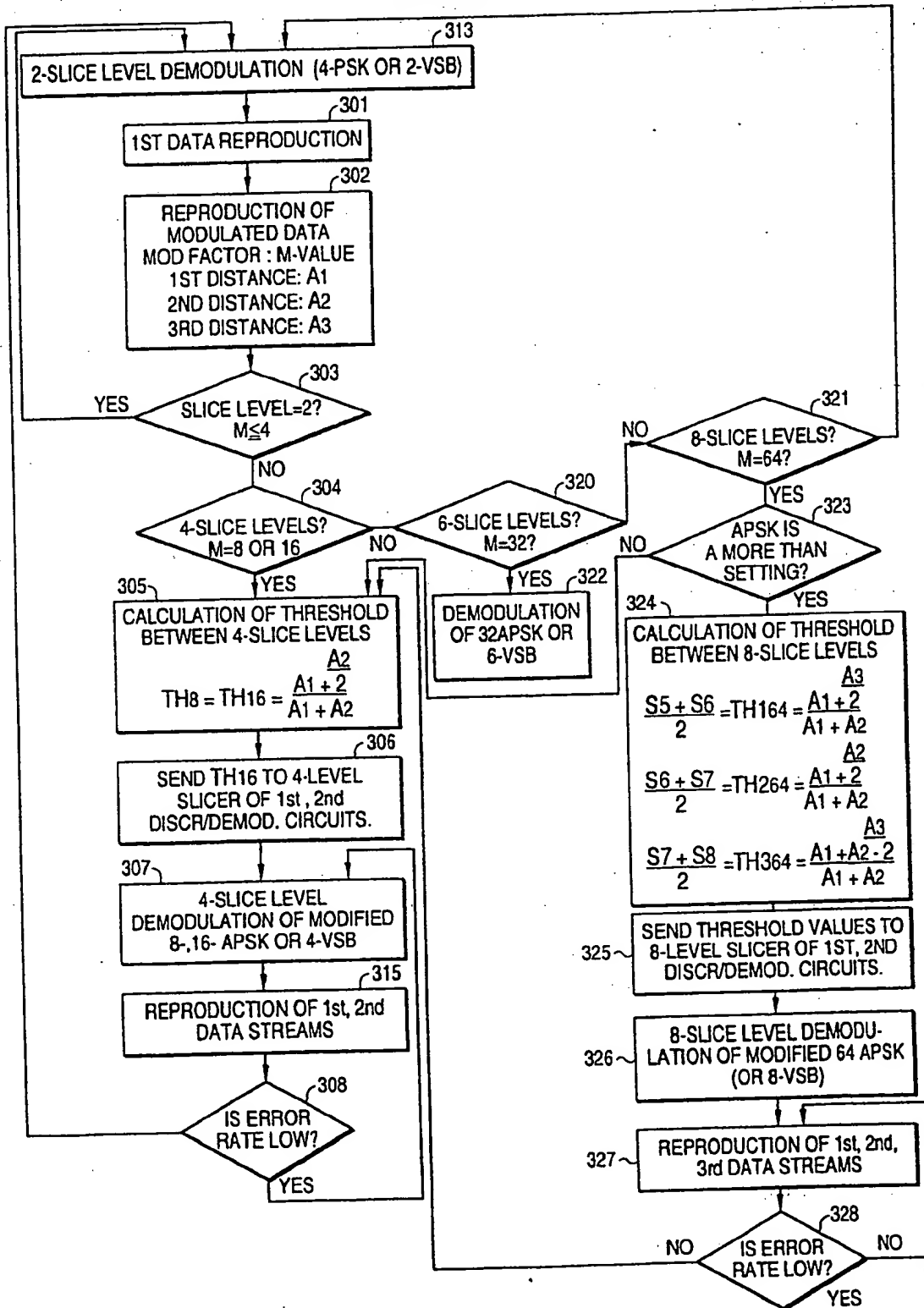


FIG. 29

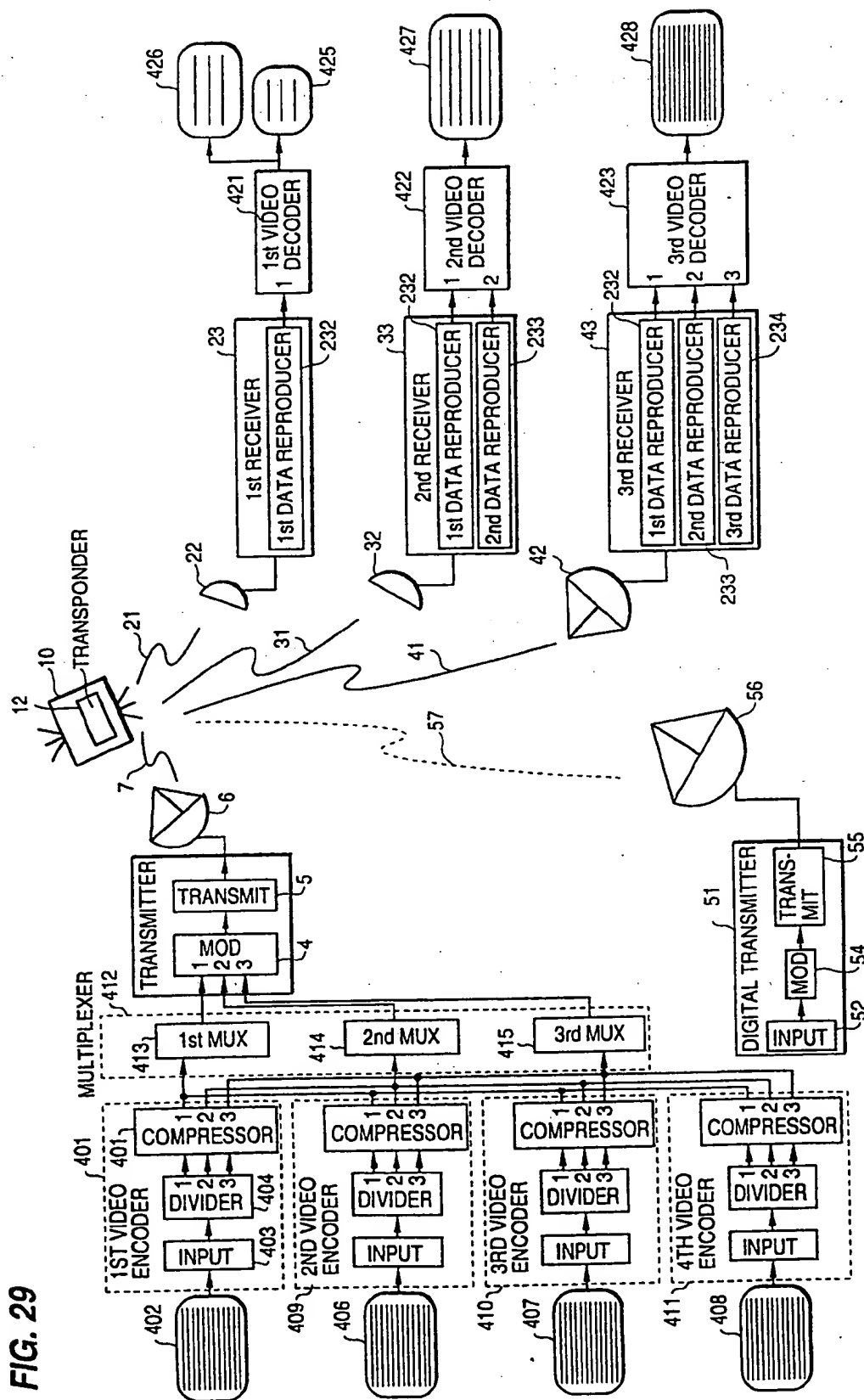
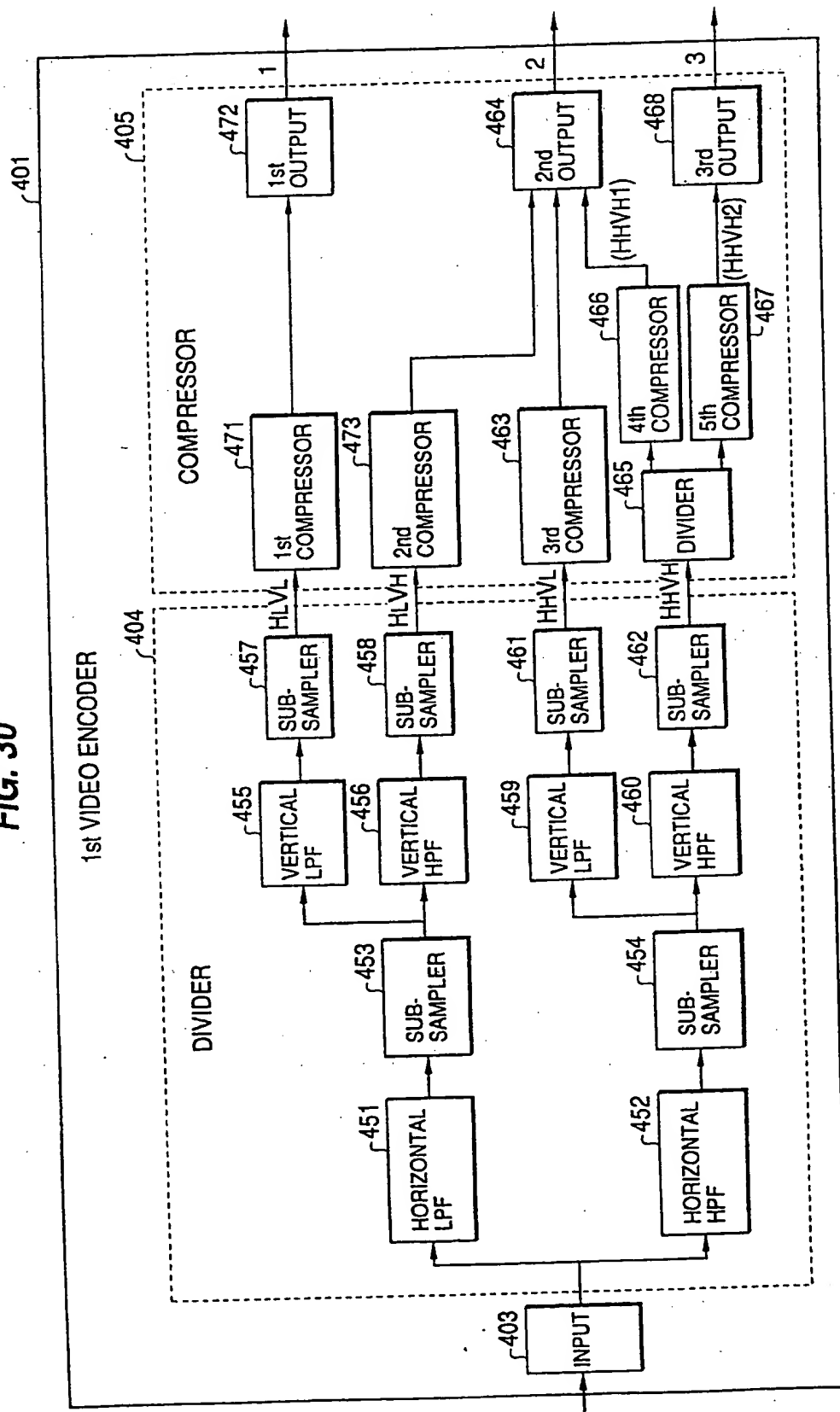


FIG. 30



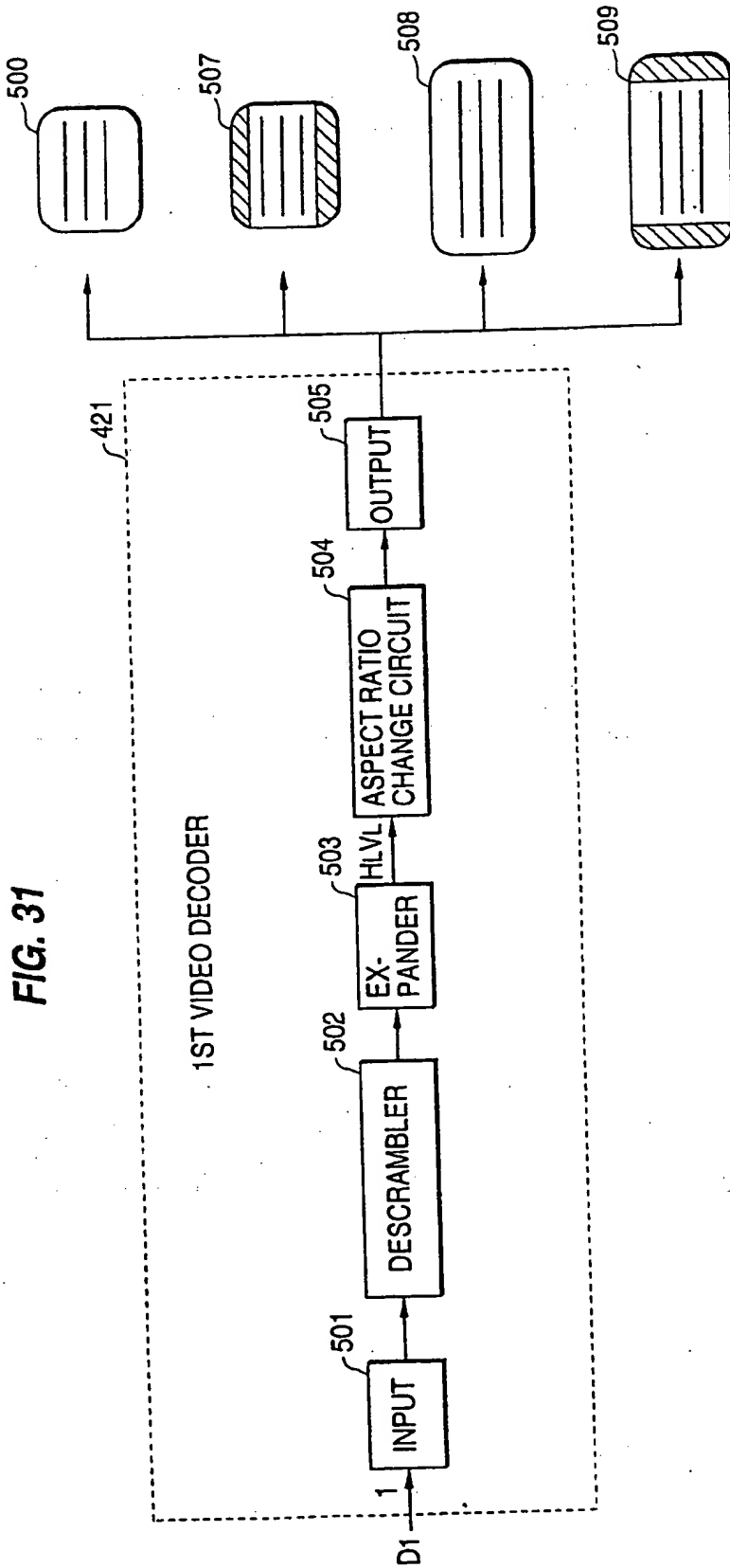


FIG. 32

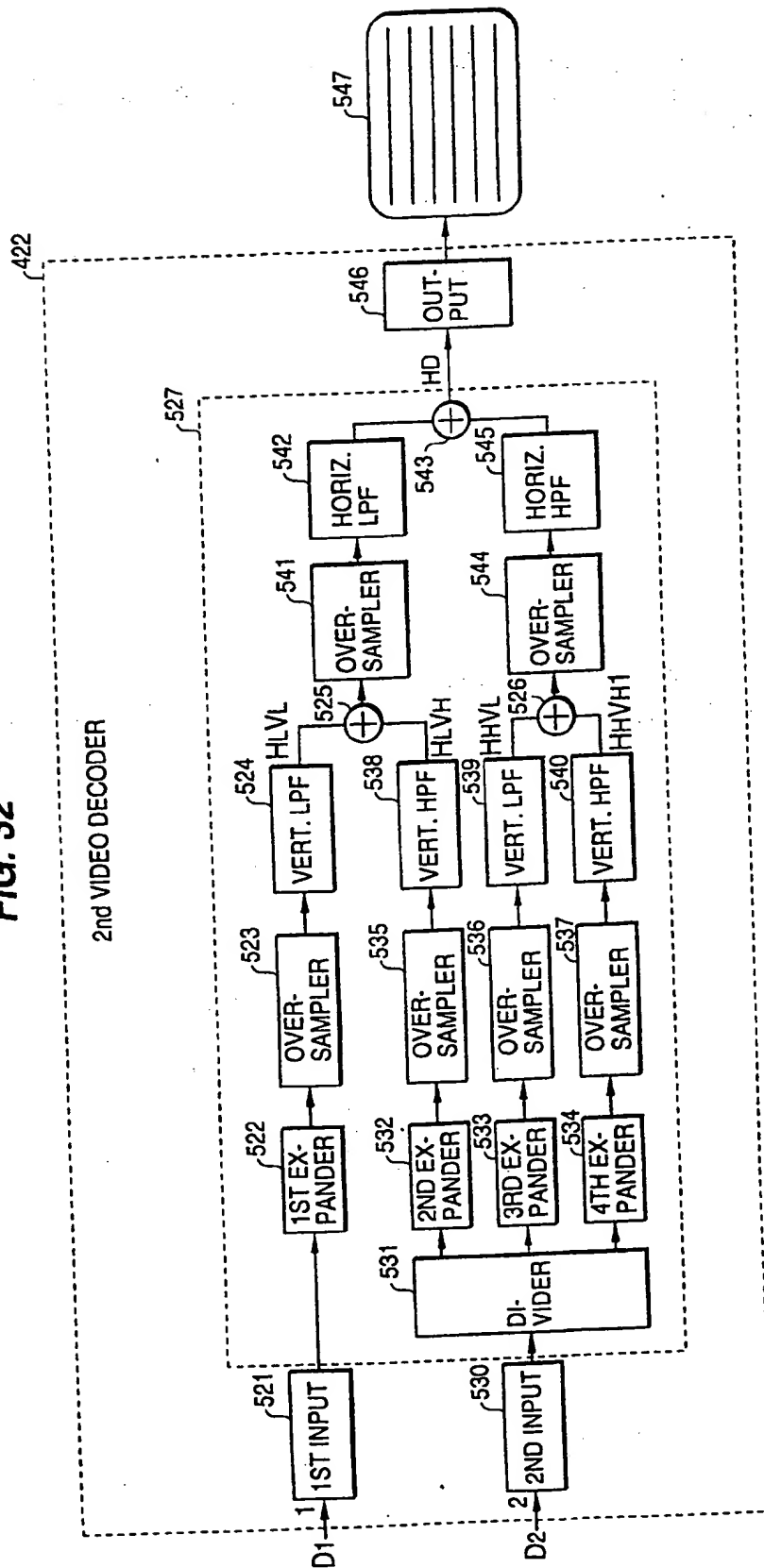


FIG. 33

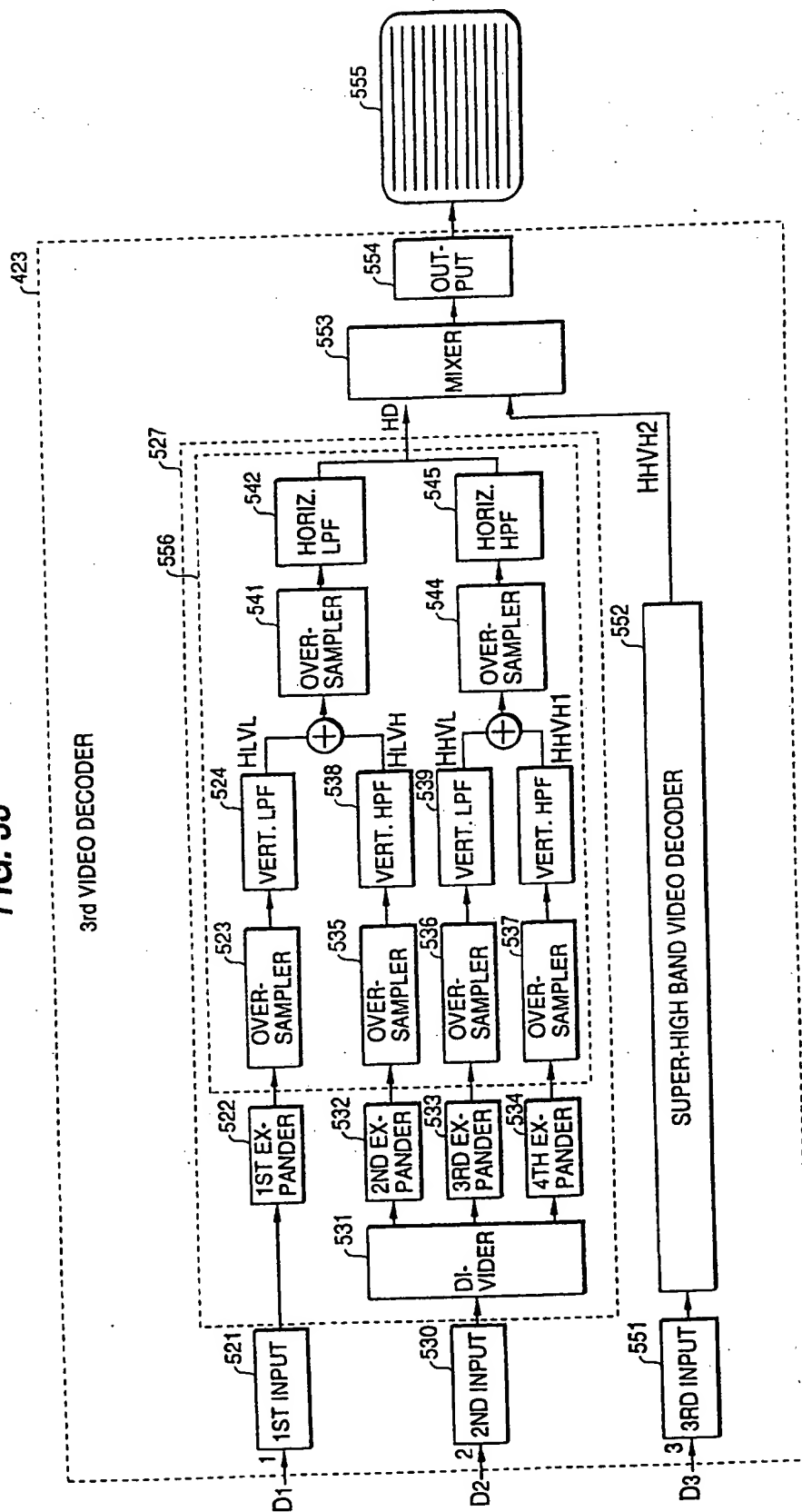


FIG. 34

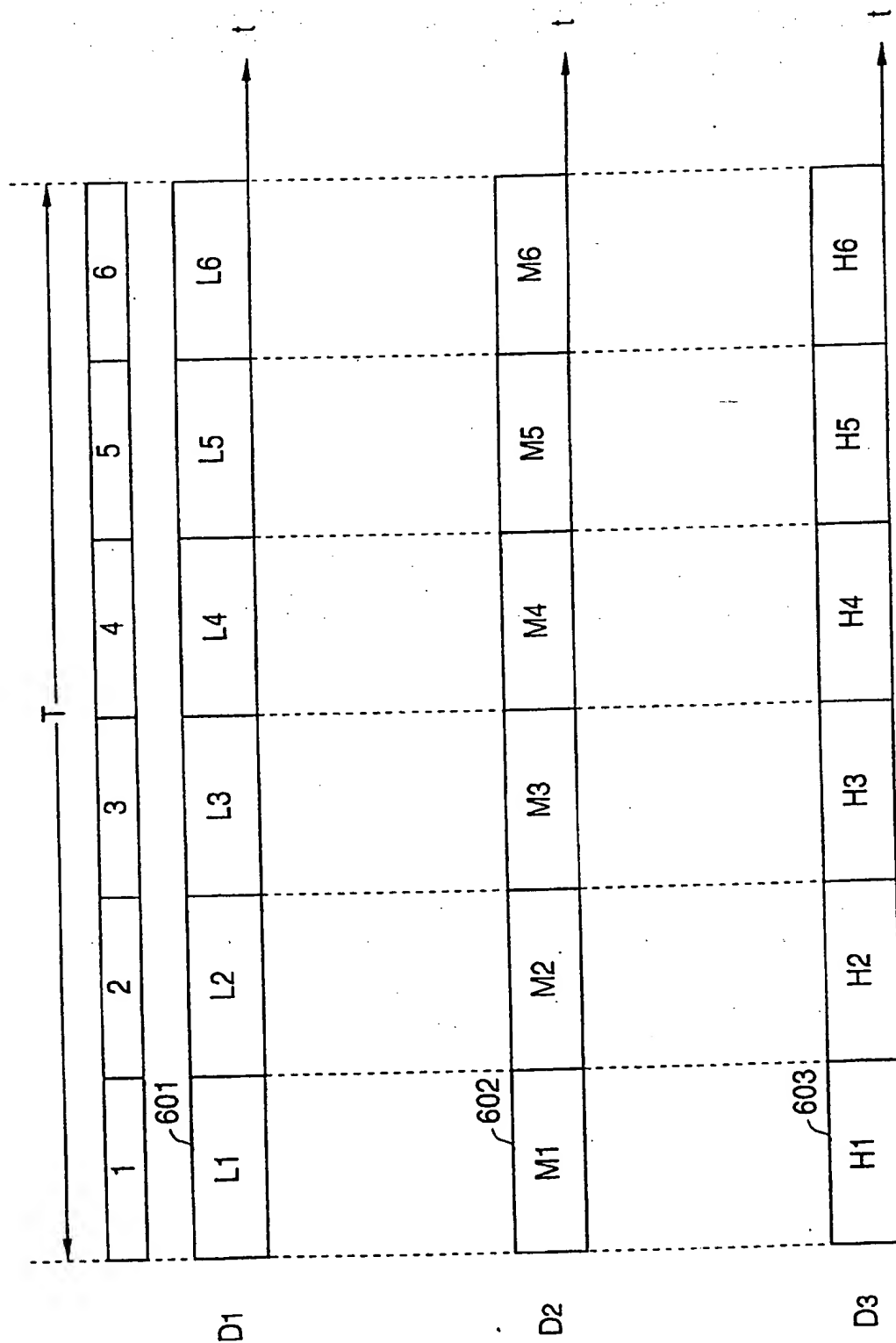


FIG. 35

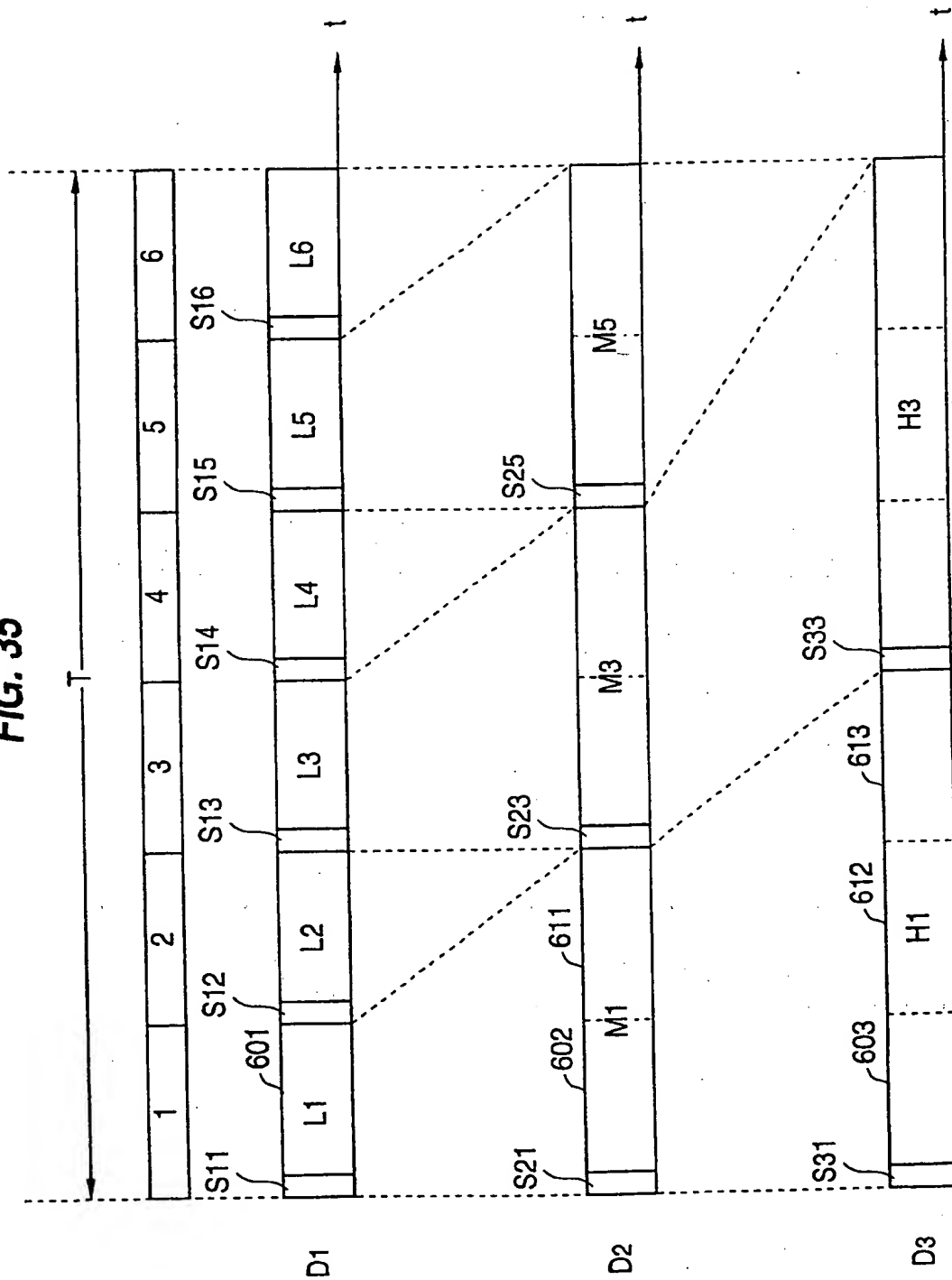


FIG. 36

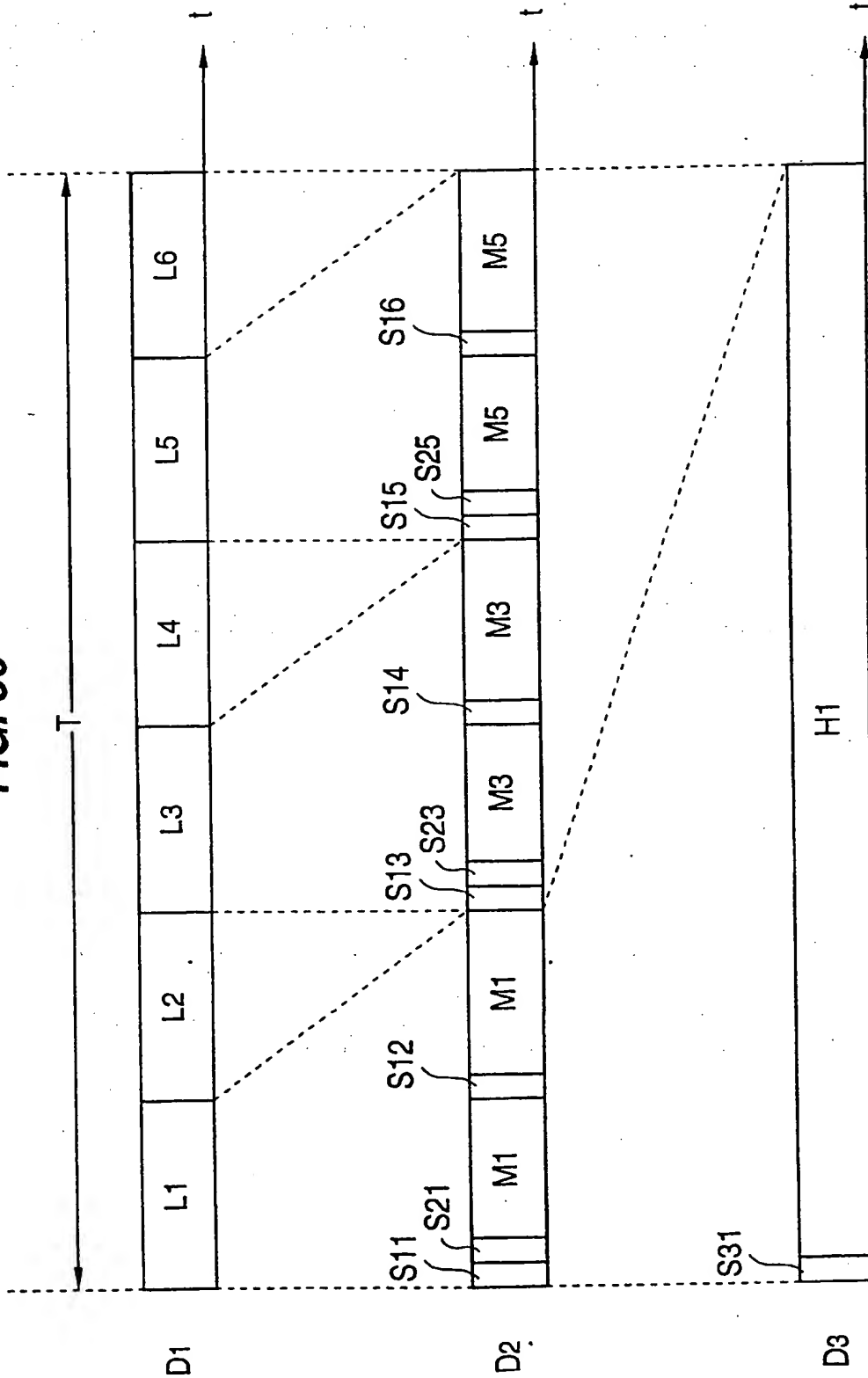


FIG. 37

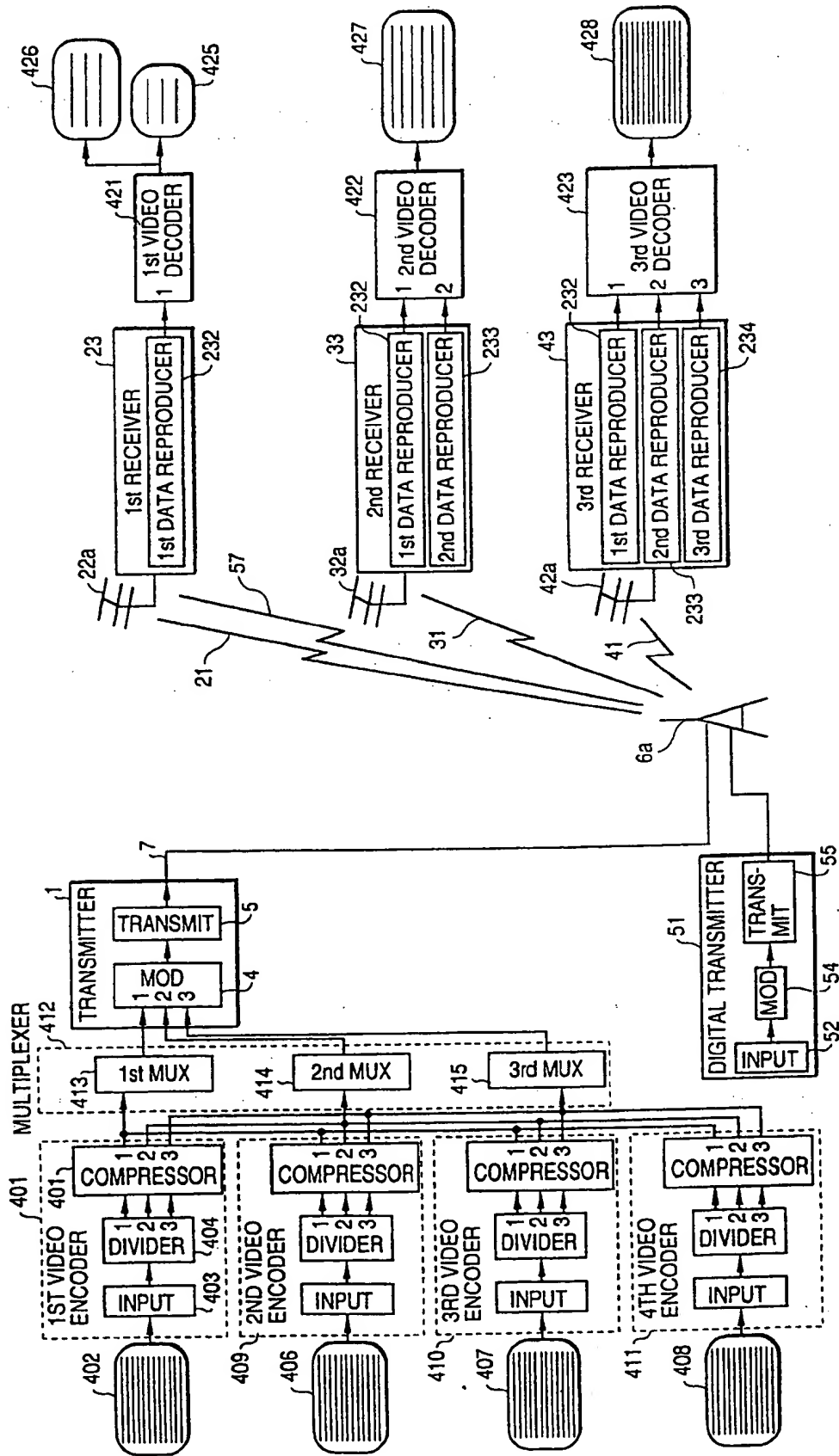


FIG. 38

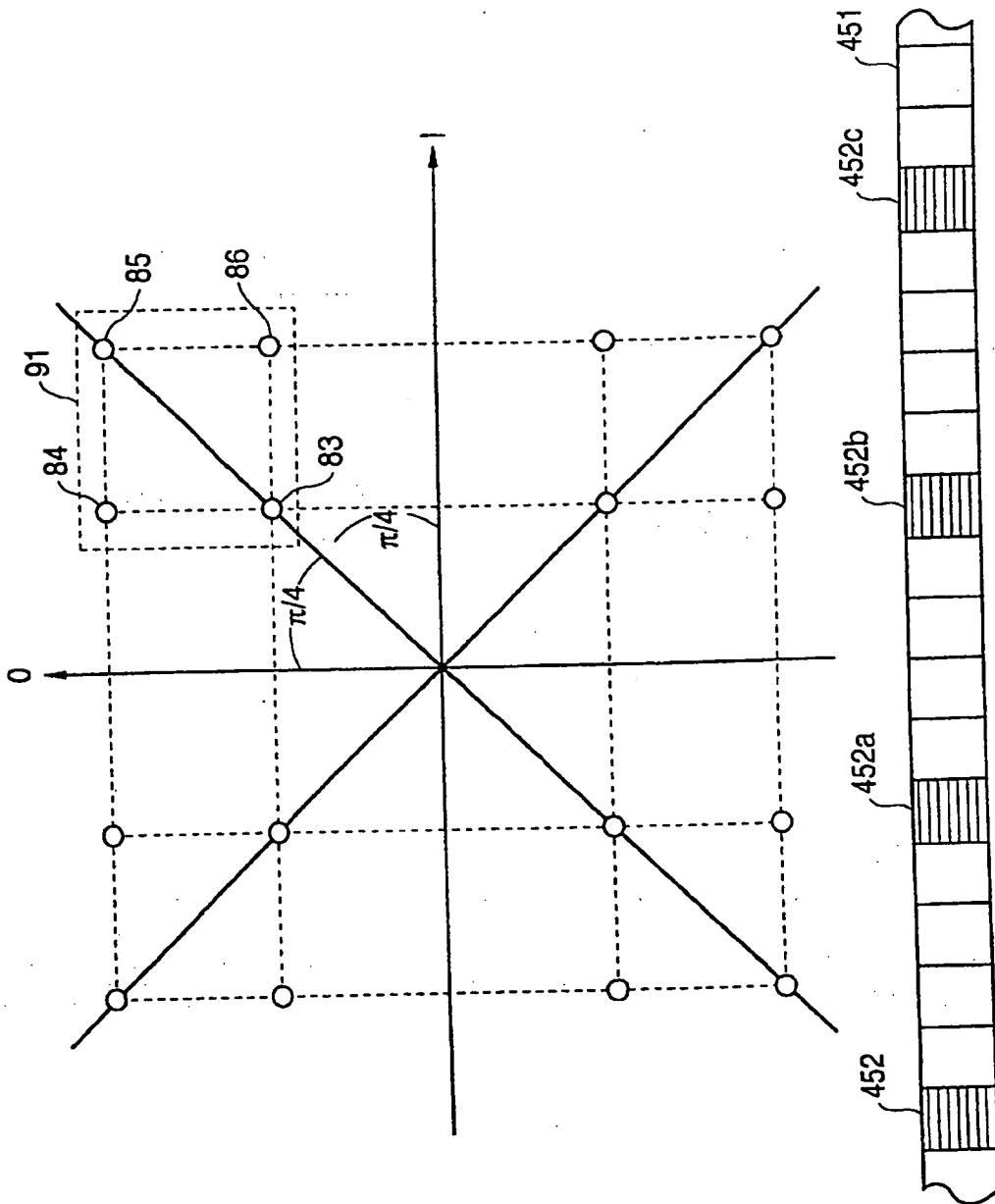


FIG. 39

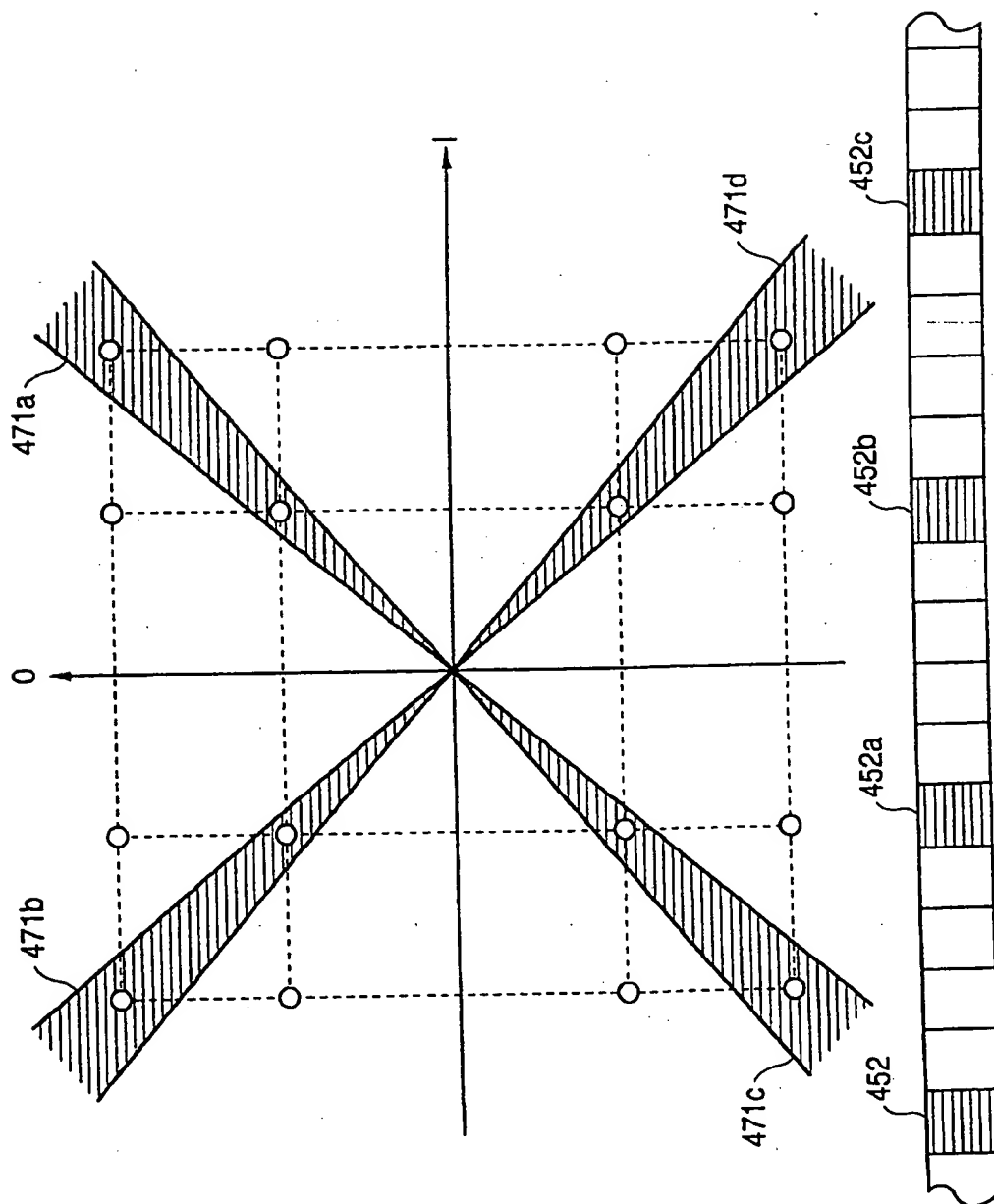


FIG. 40

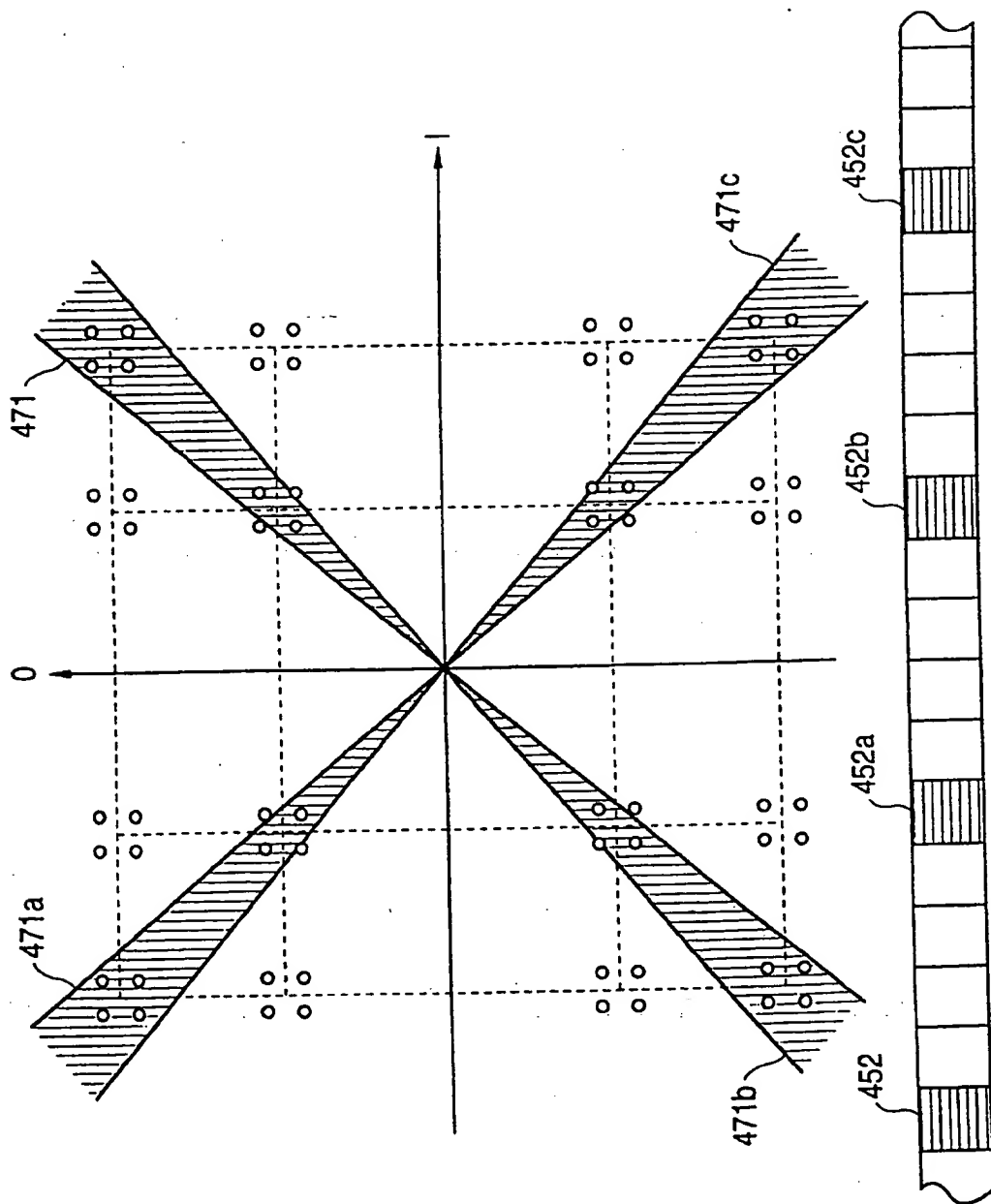


FIG. 41

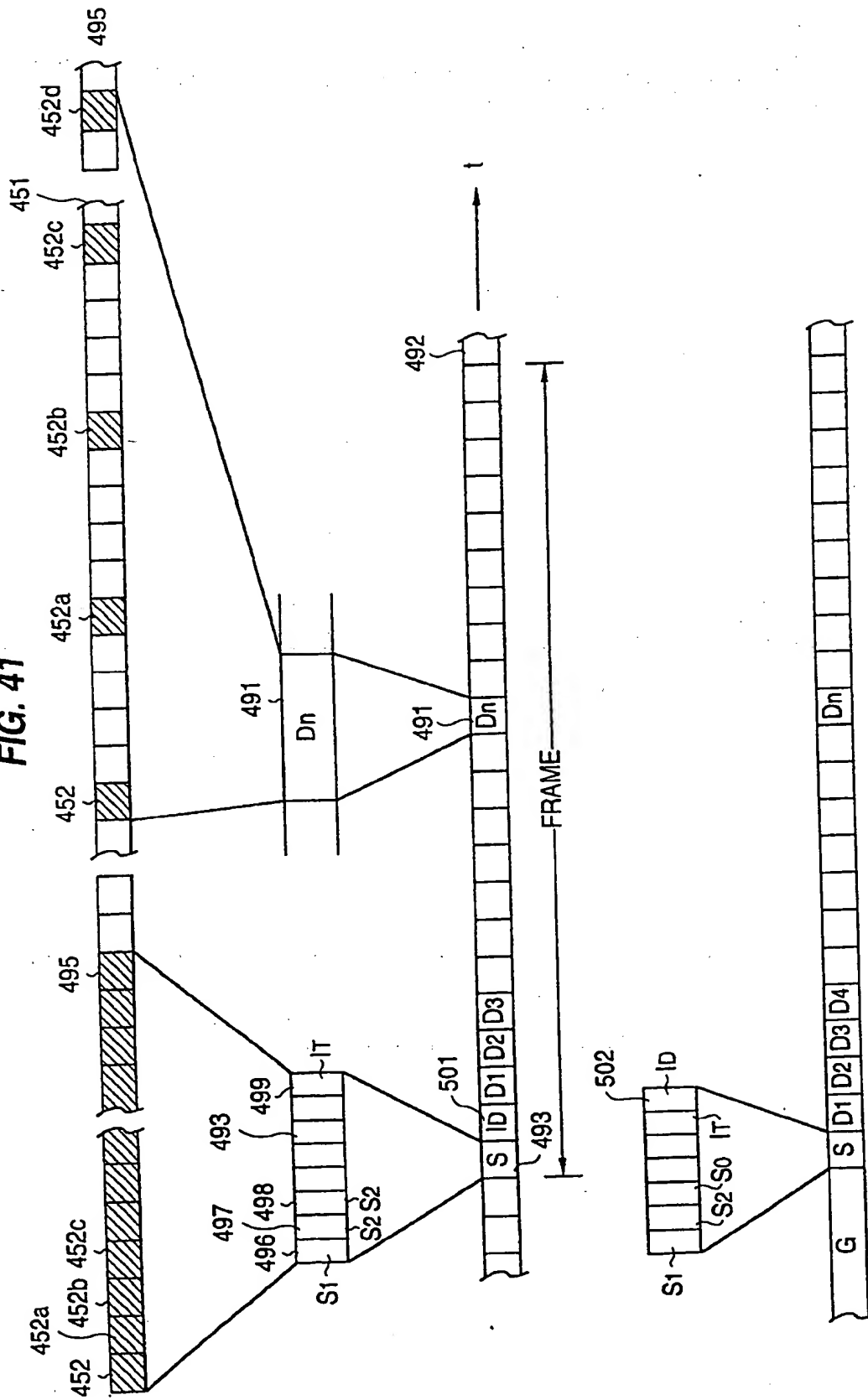


FIG. 42

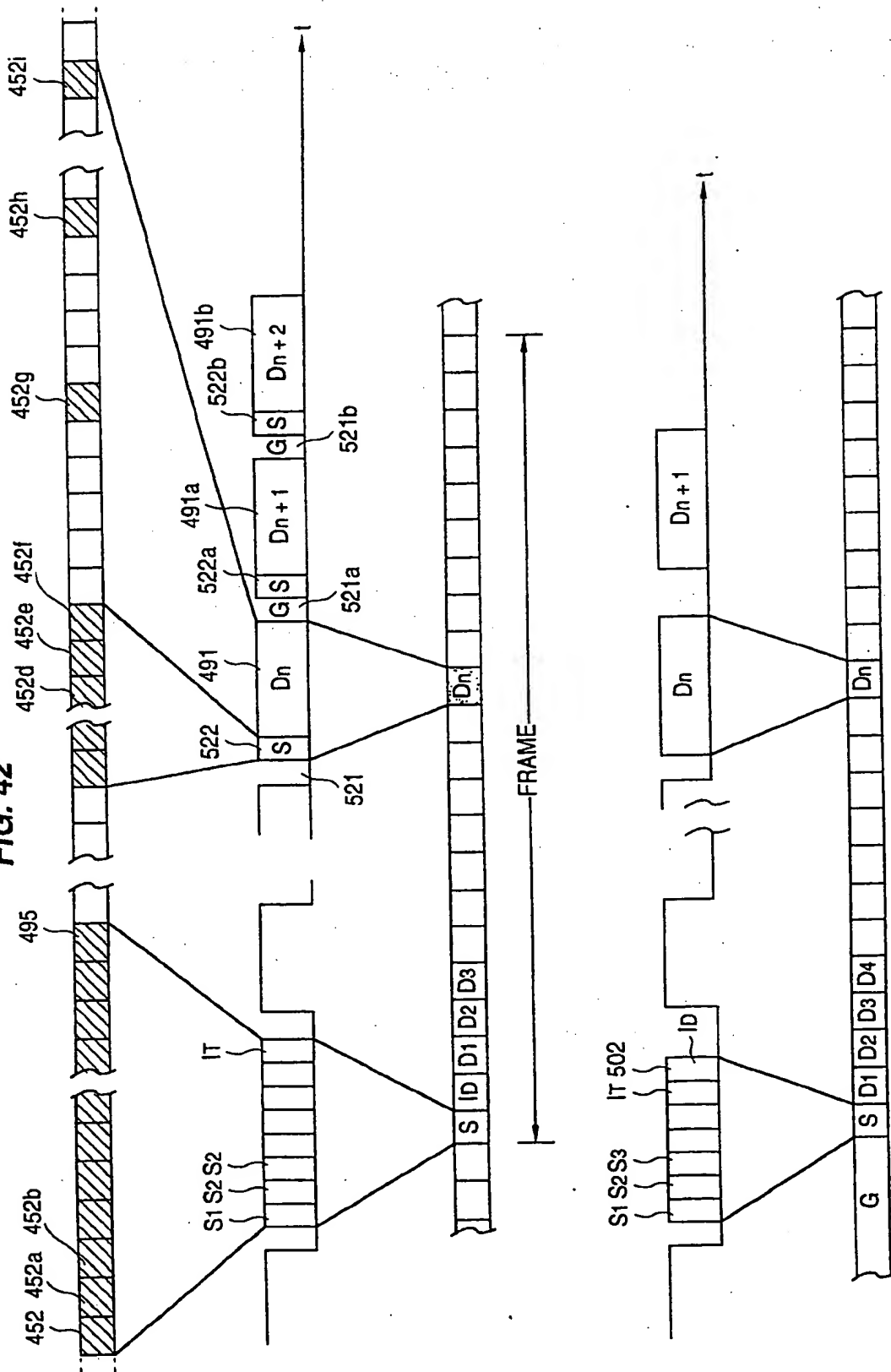


FIG. 43

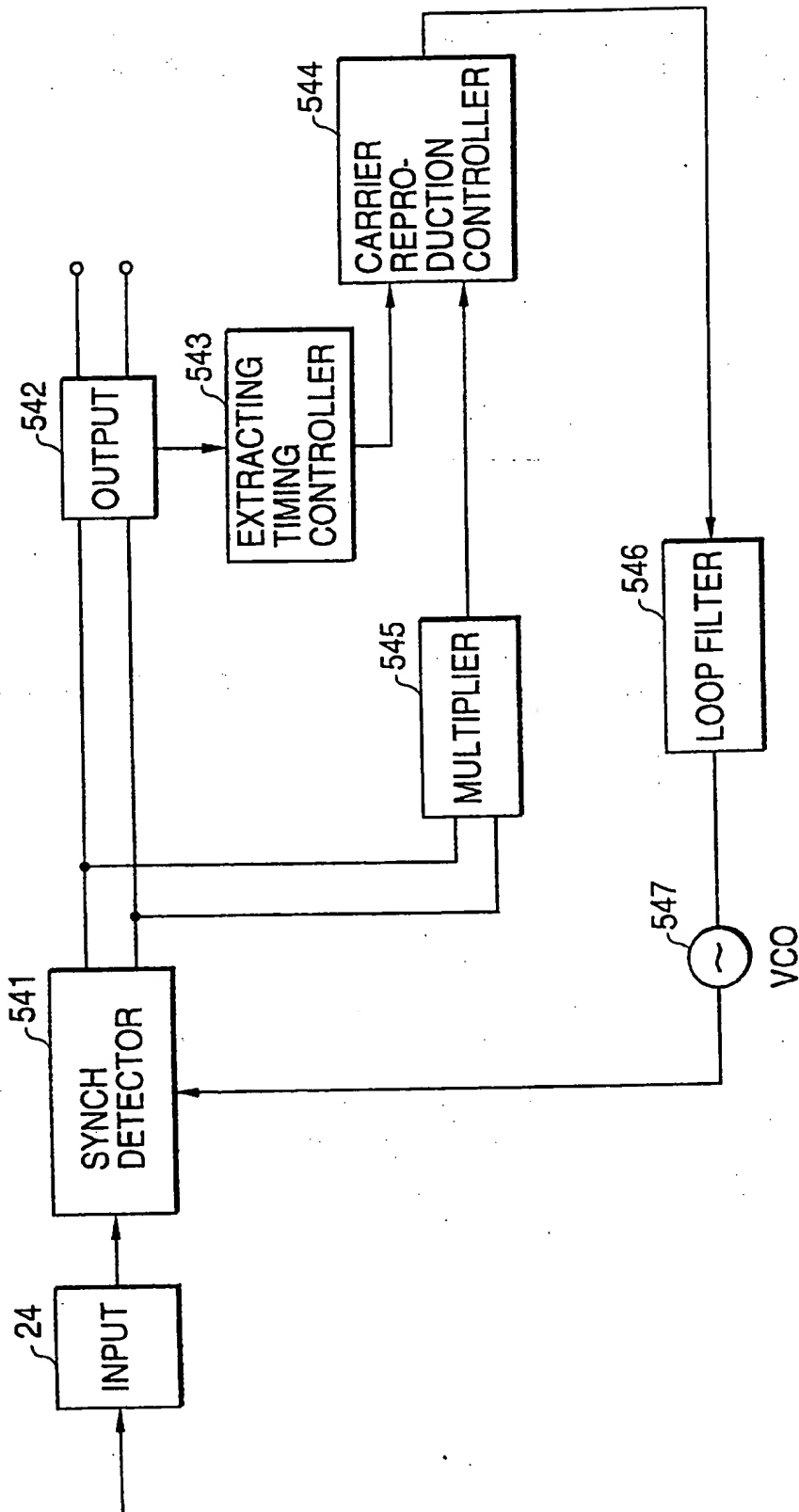


FIG. 44

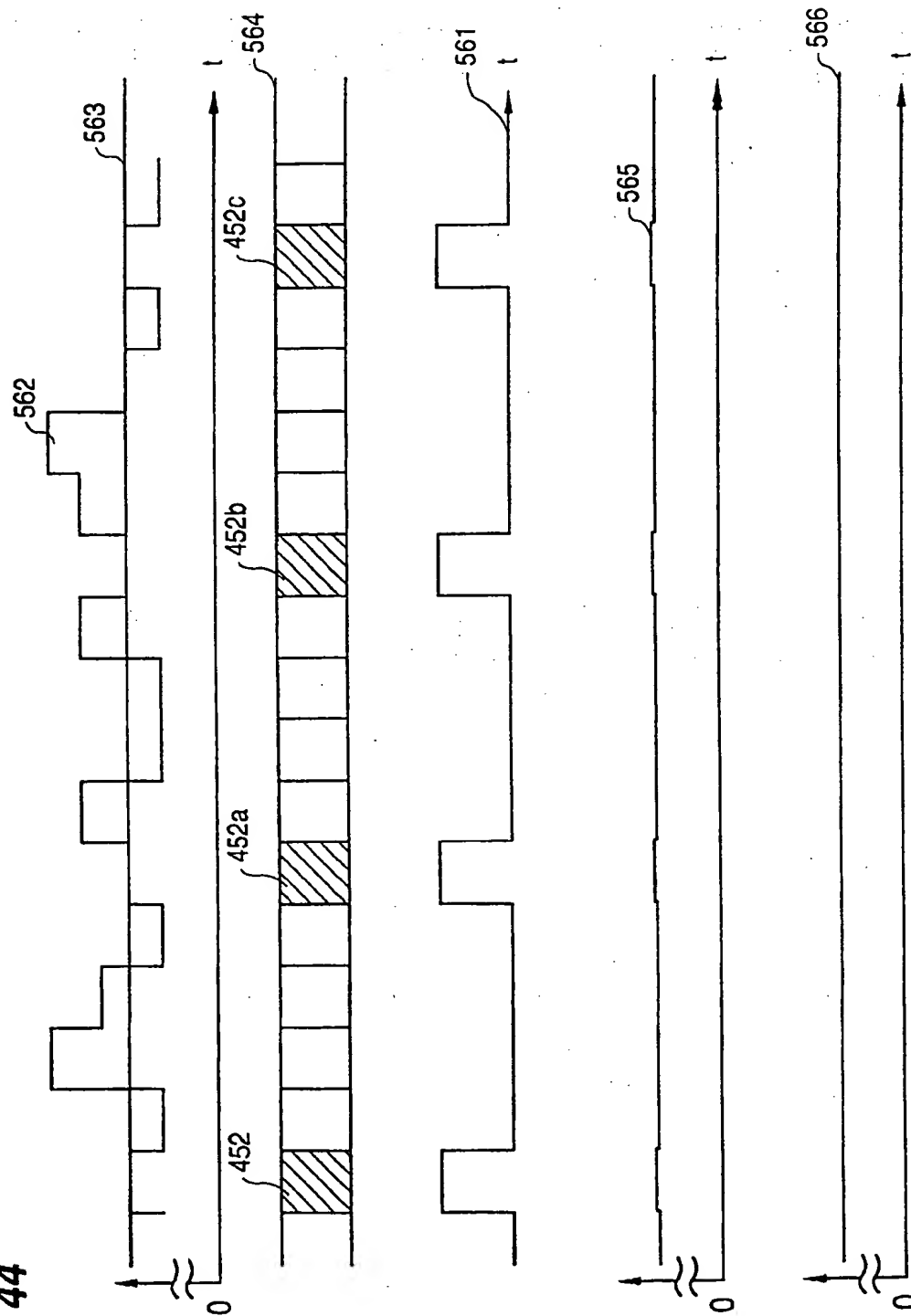


FIG. 45

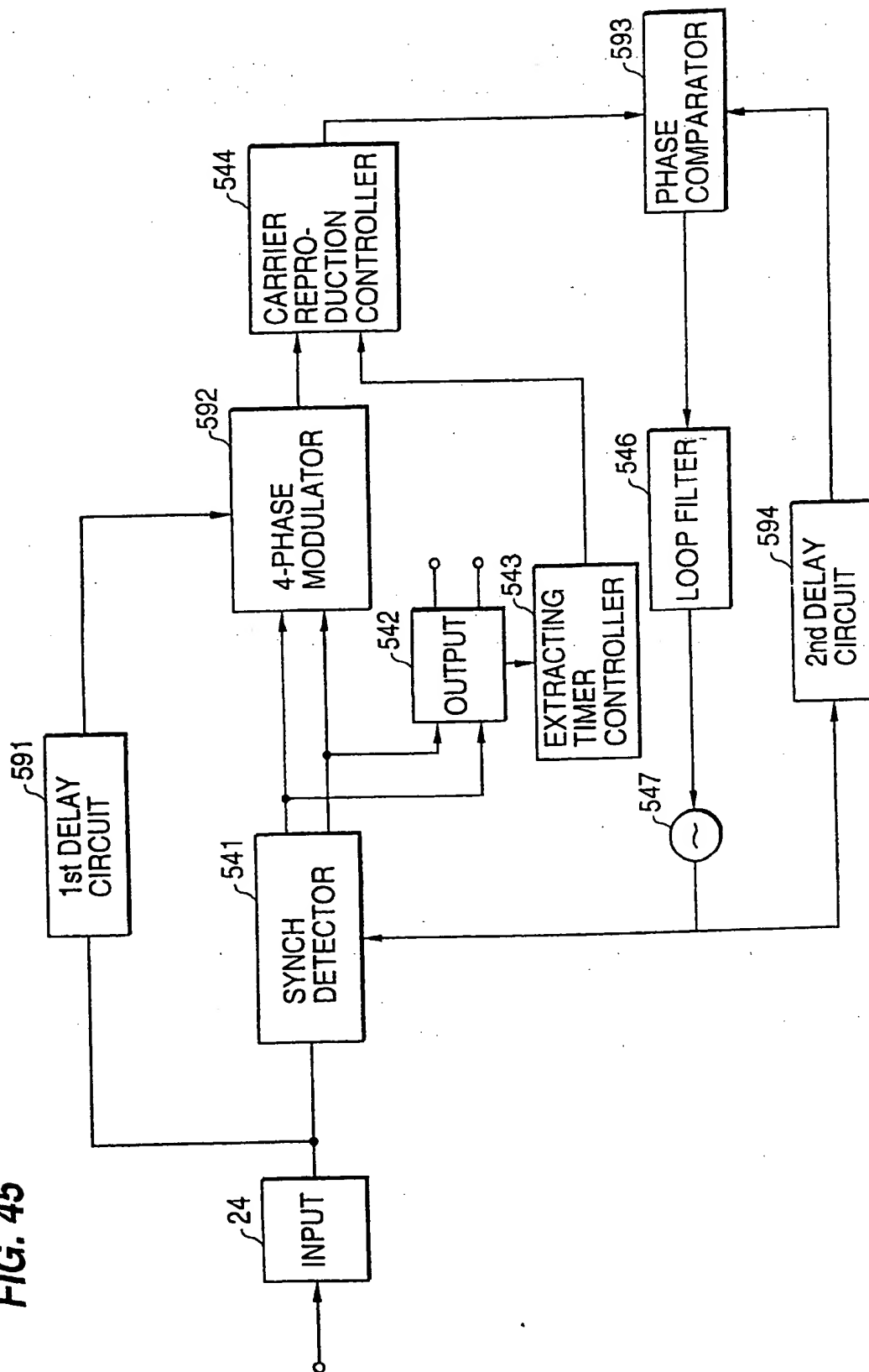


FIG. 46

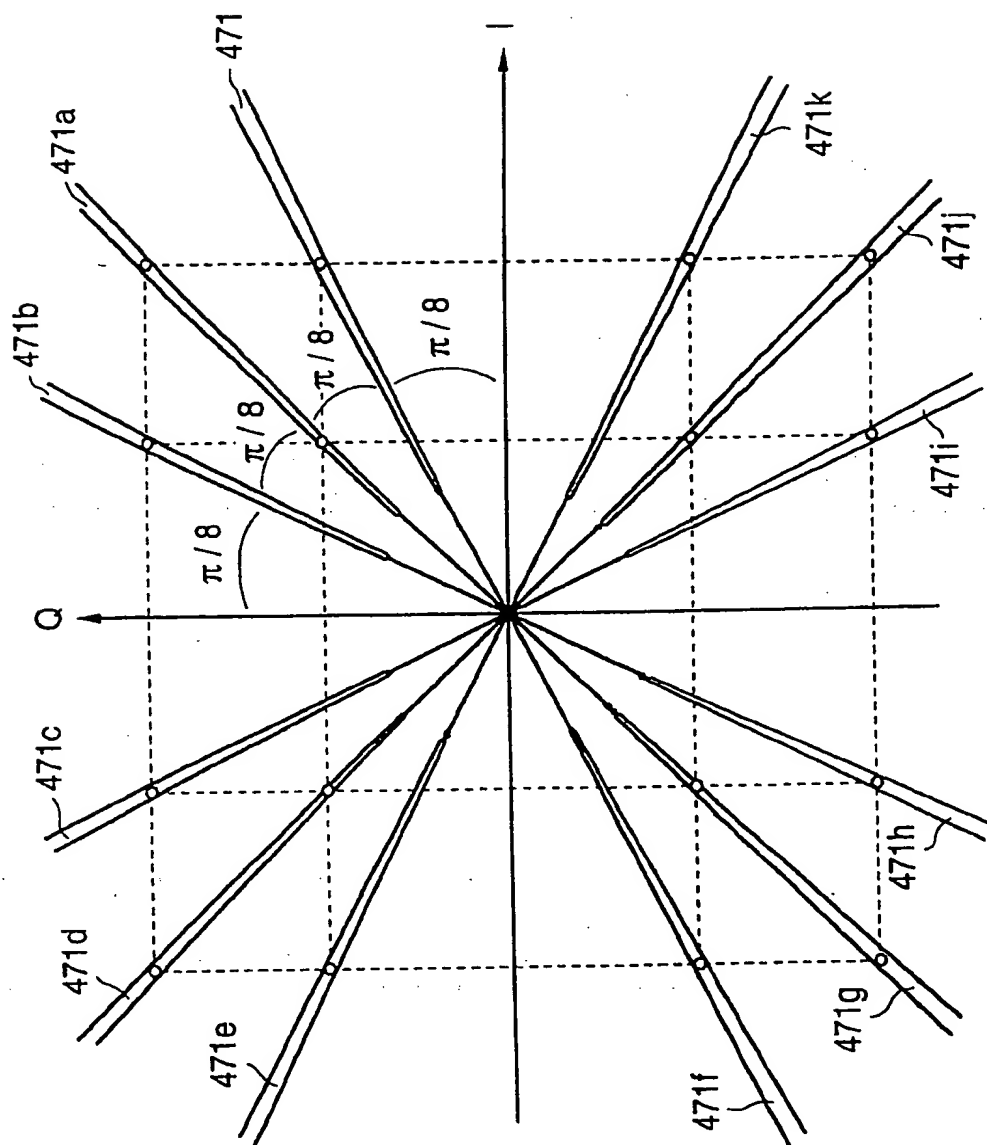


FIG. 47

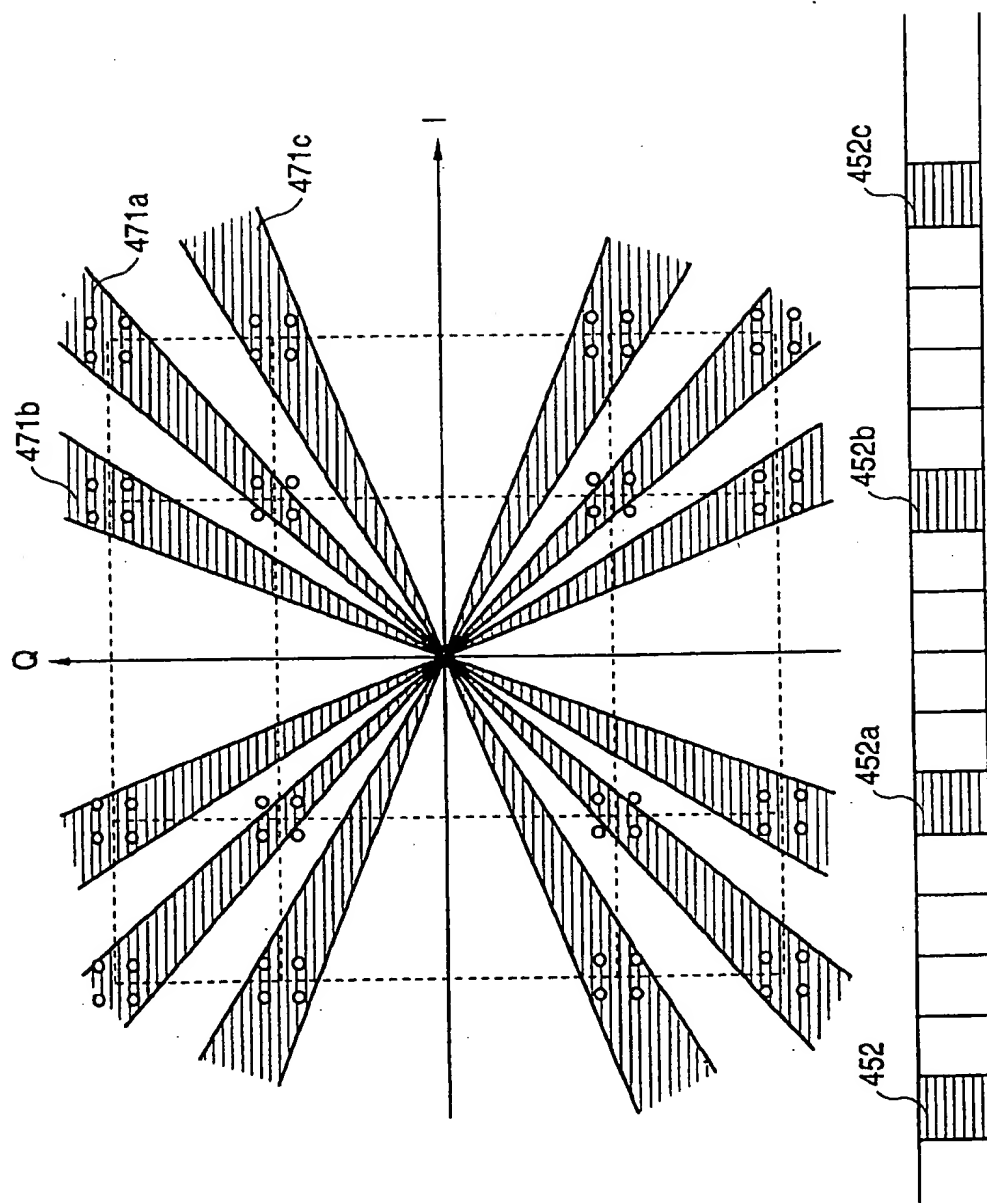


FIG. 48

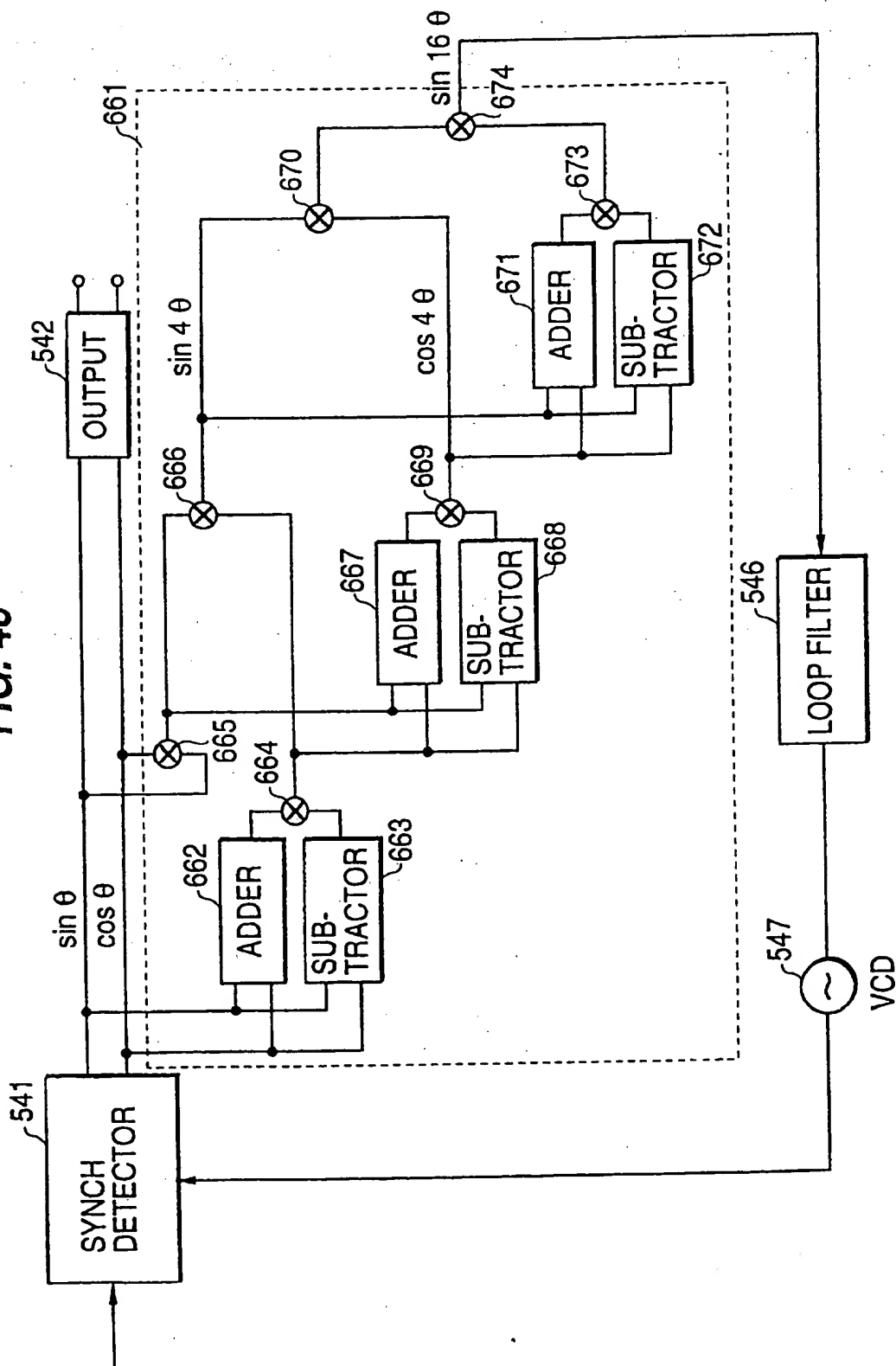


FIG. 50

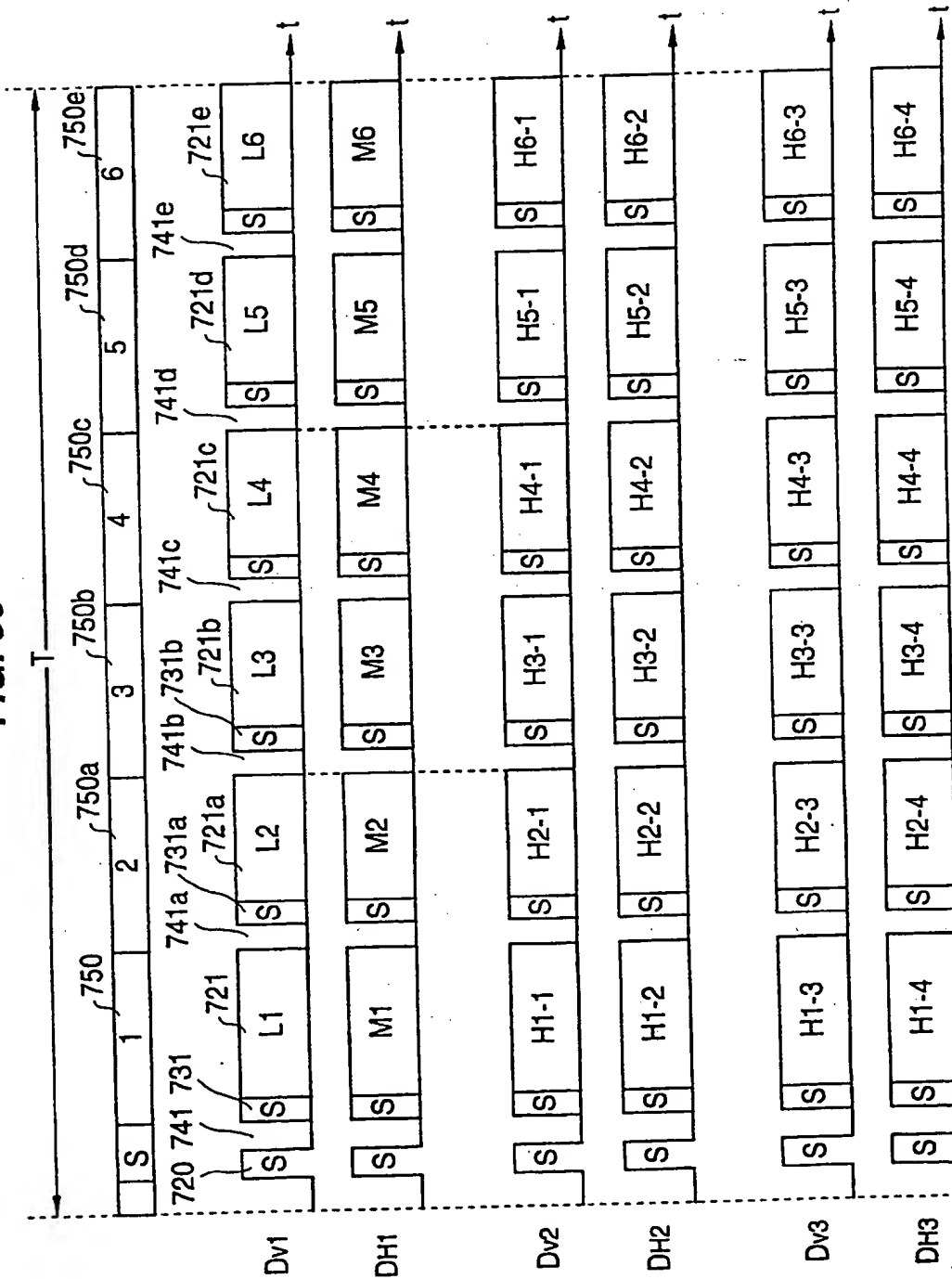


FIG. 51

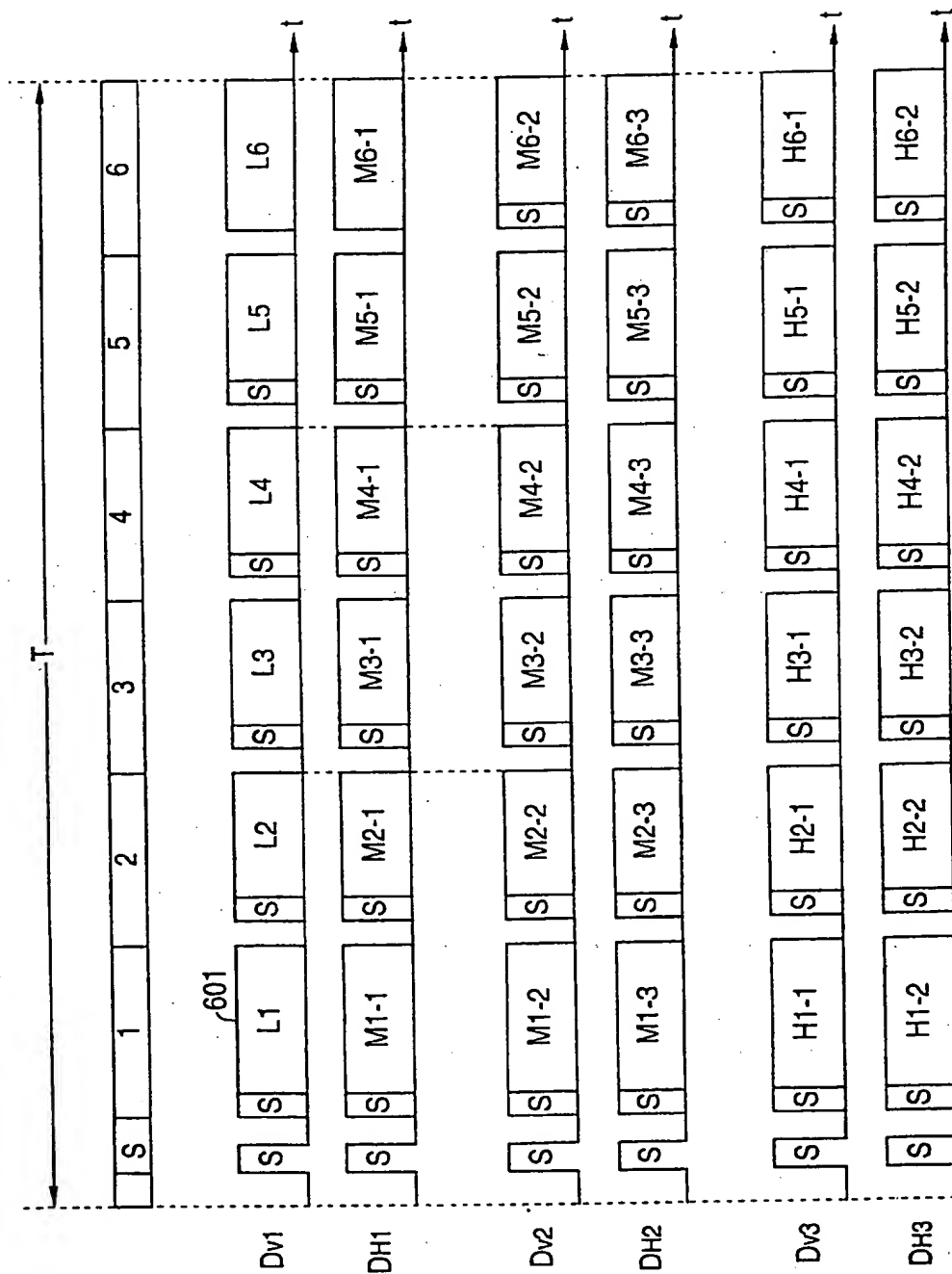


FIG. 52

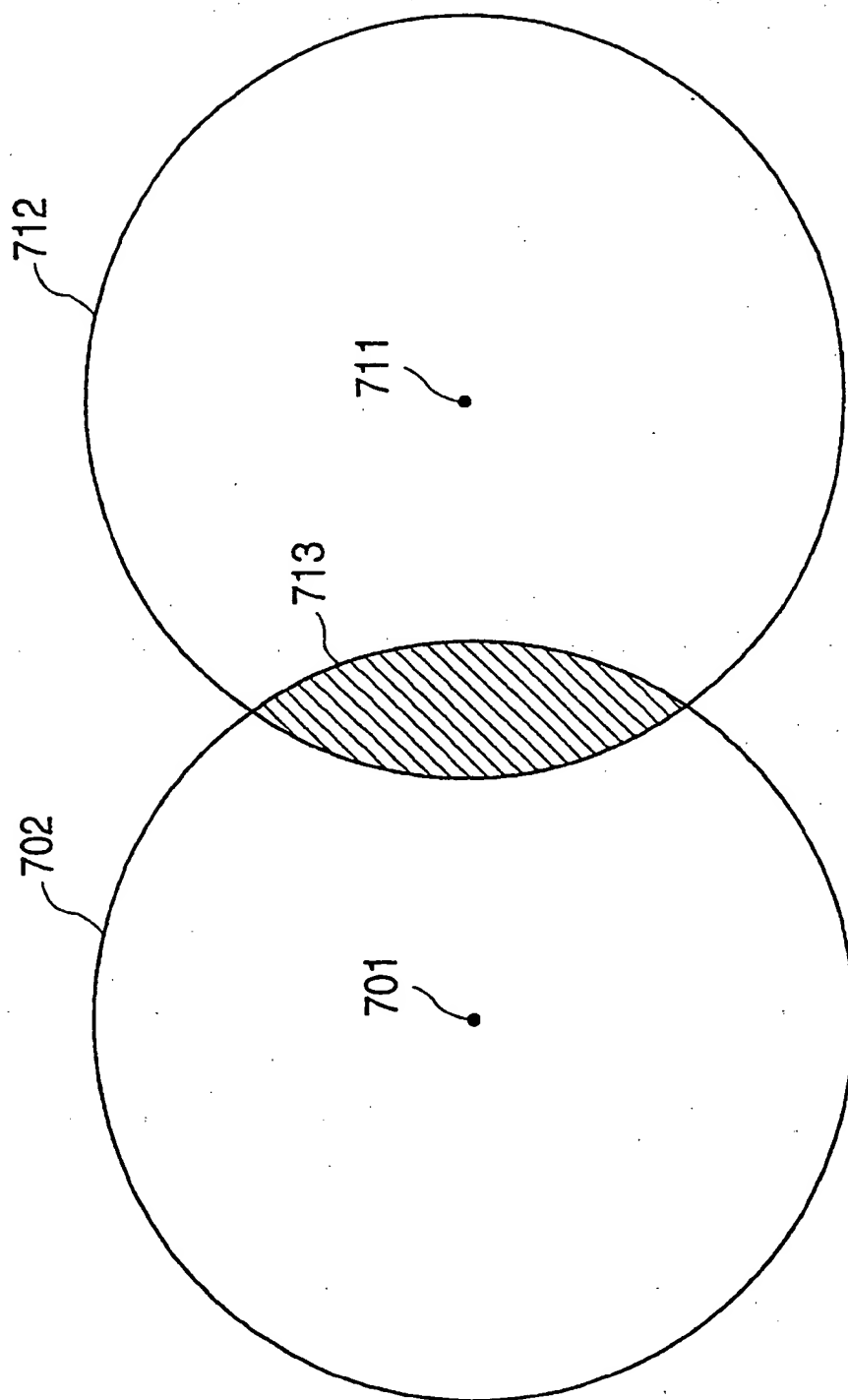


FIG. 53

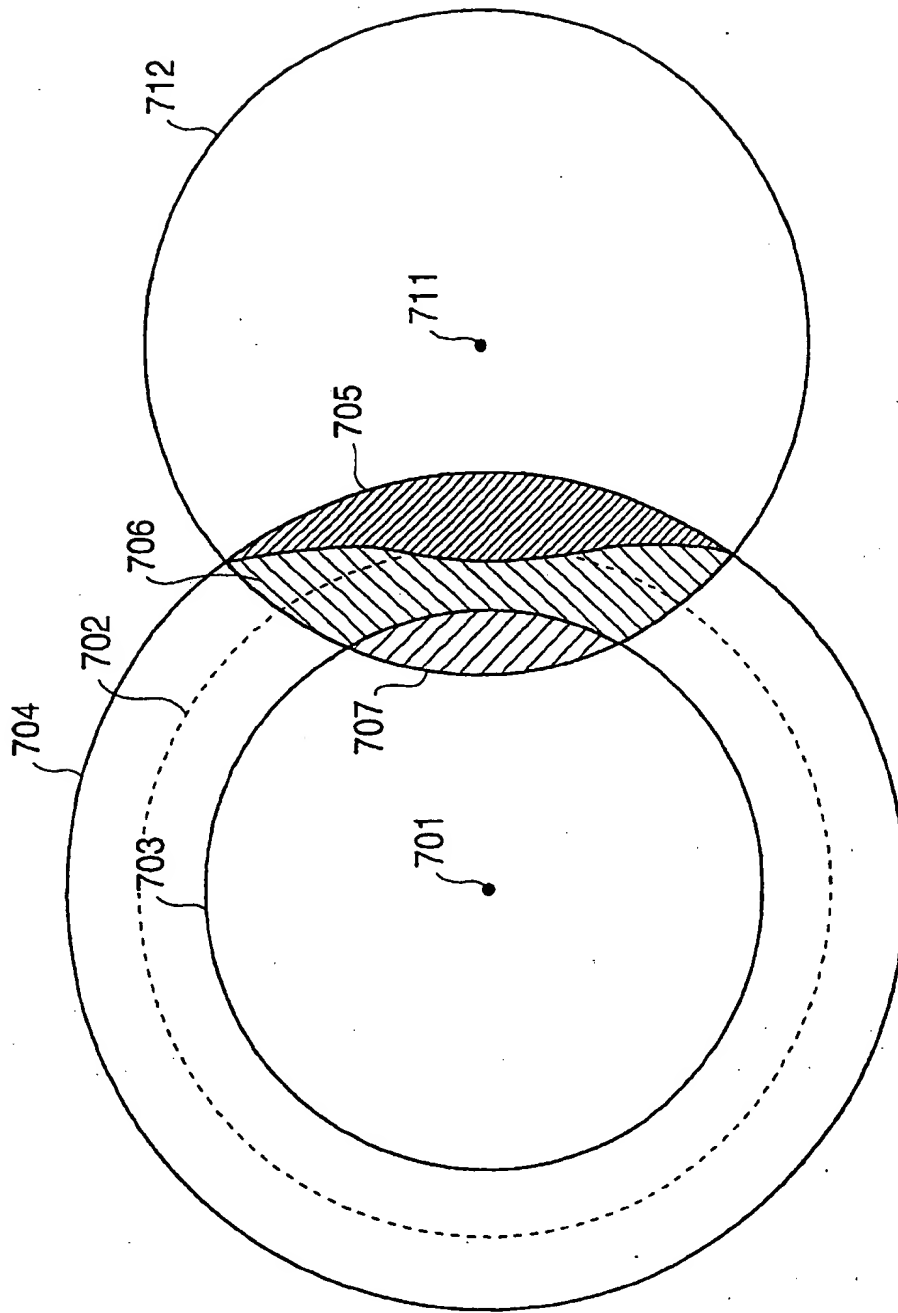


FIG. 54

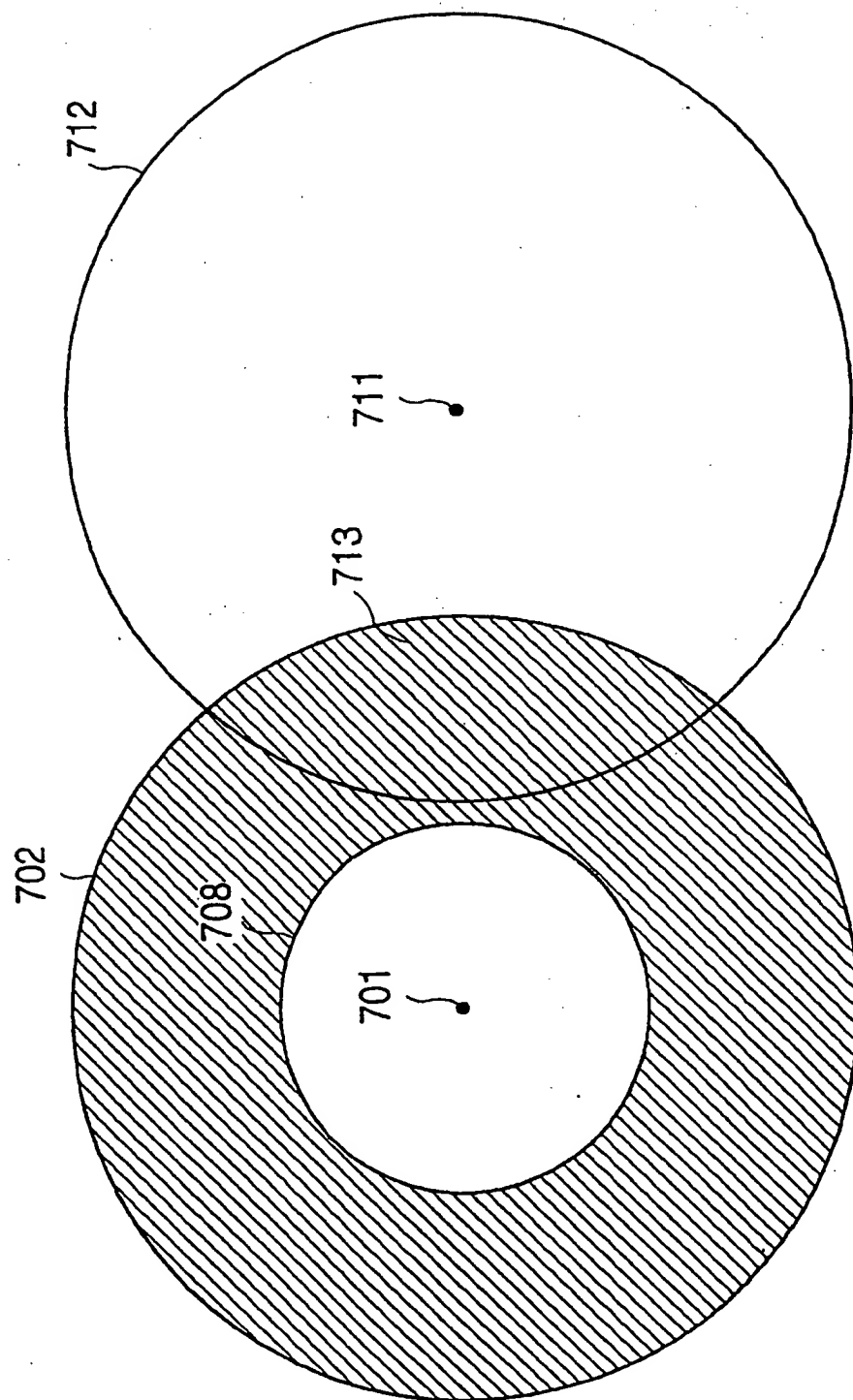


FIG. 55

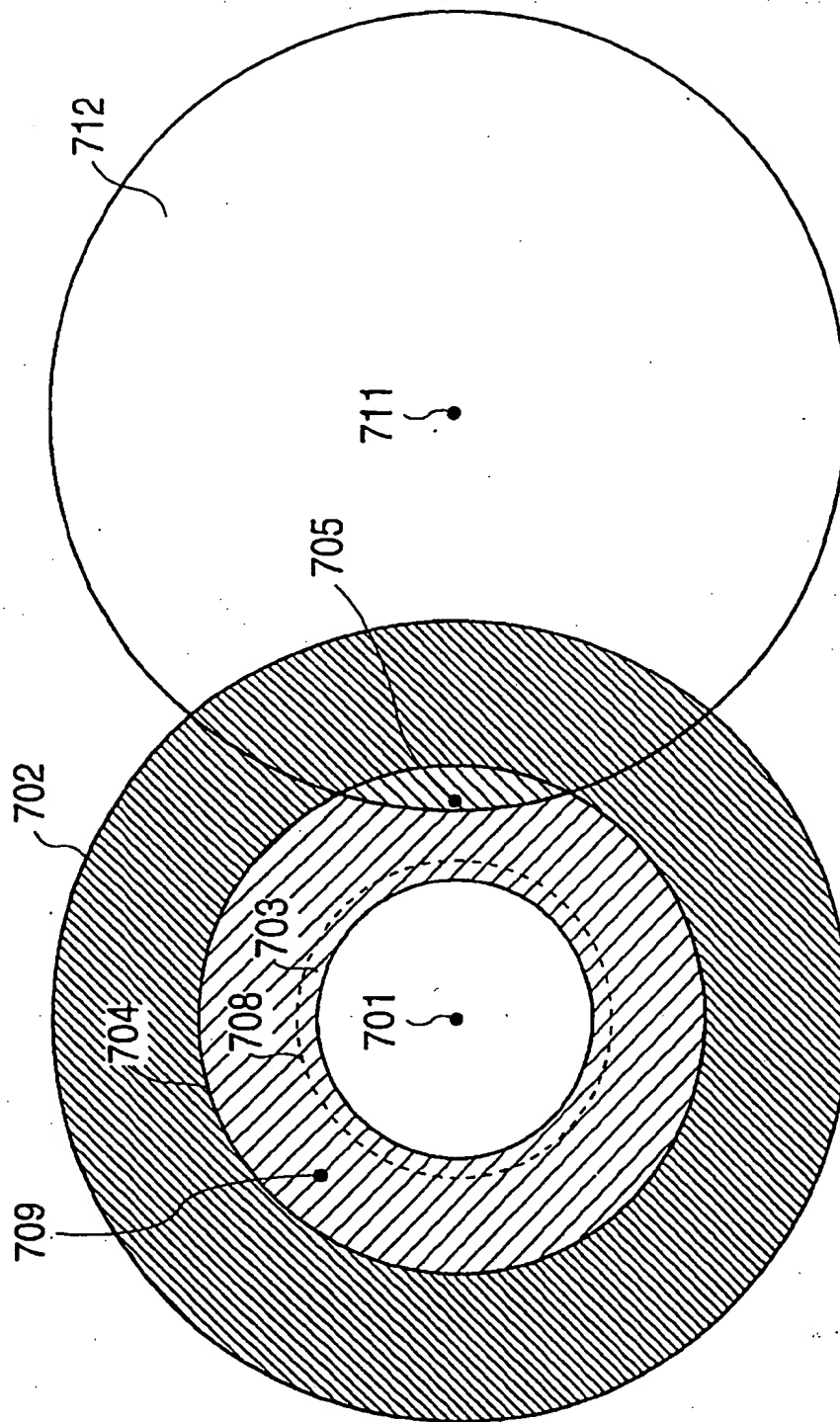


FIG. 56

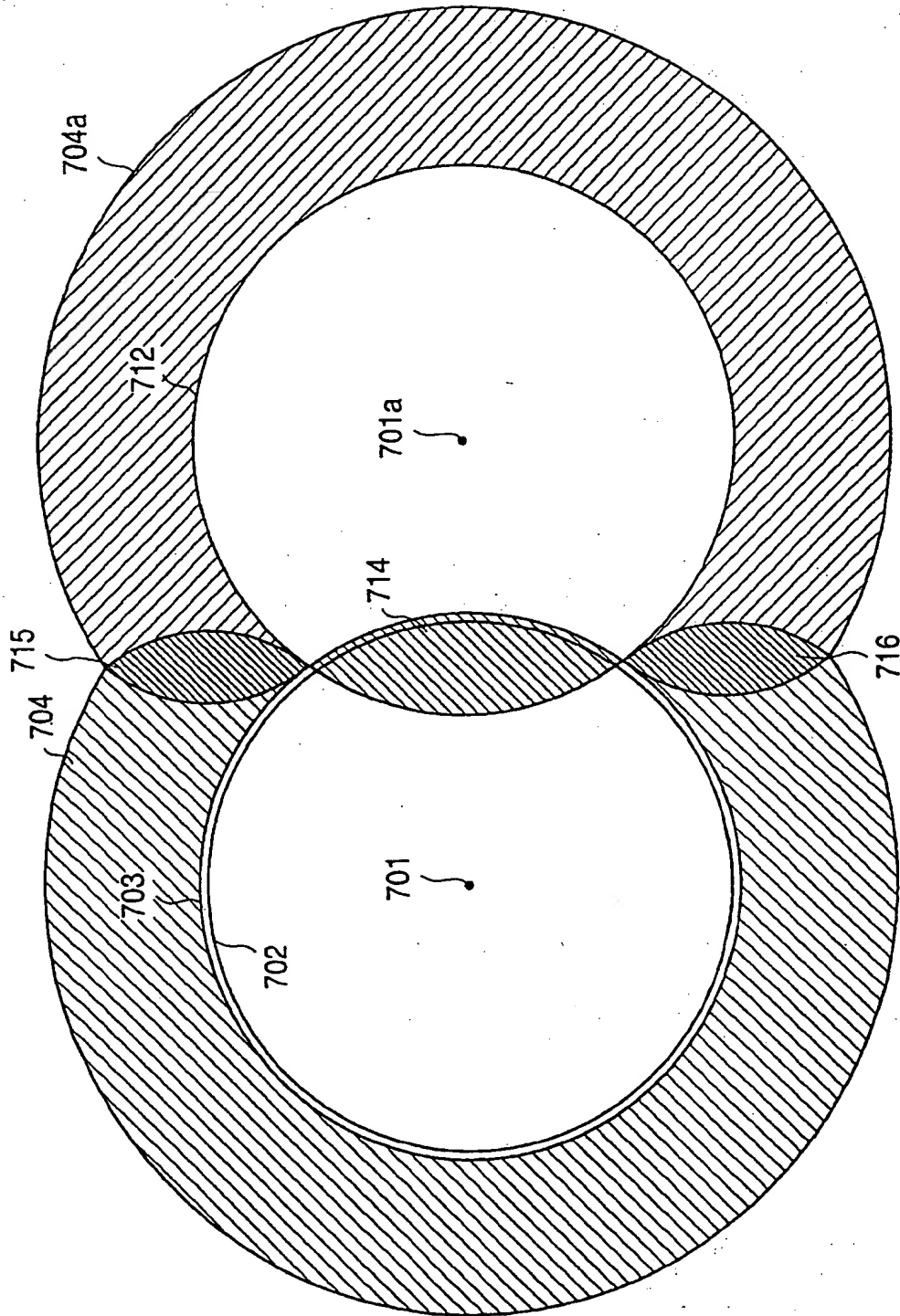


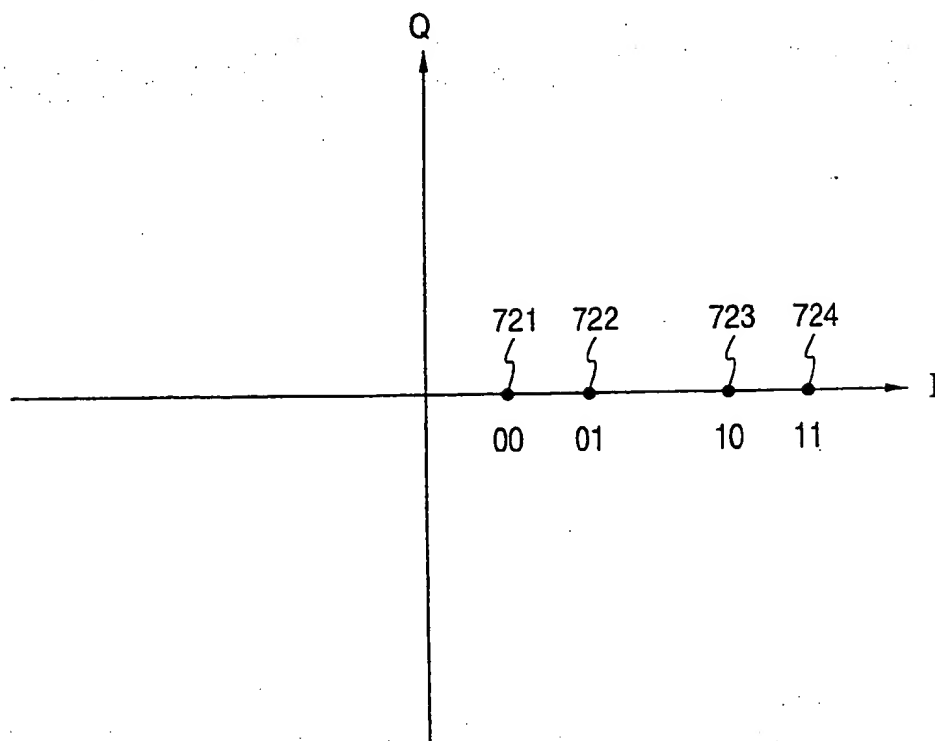
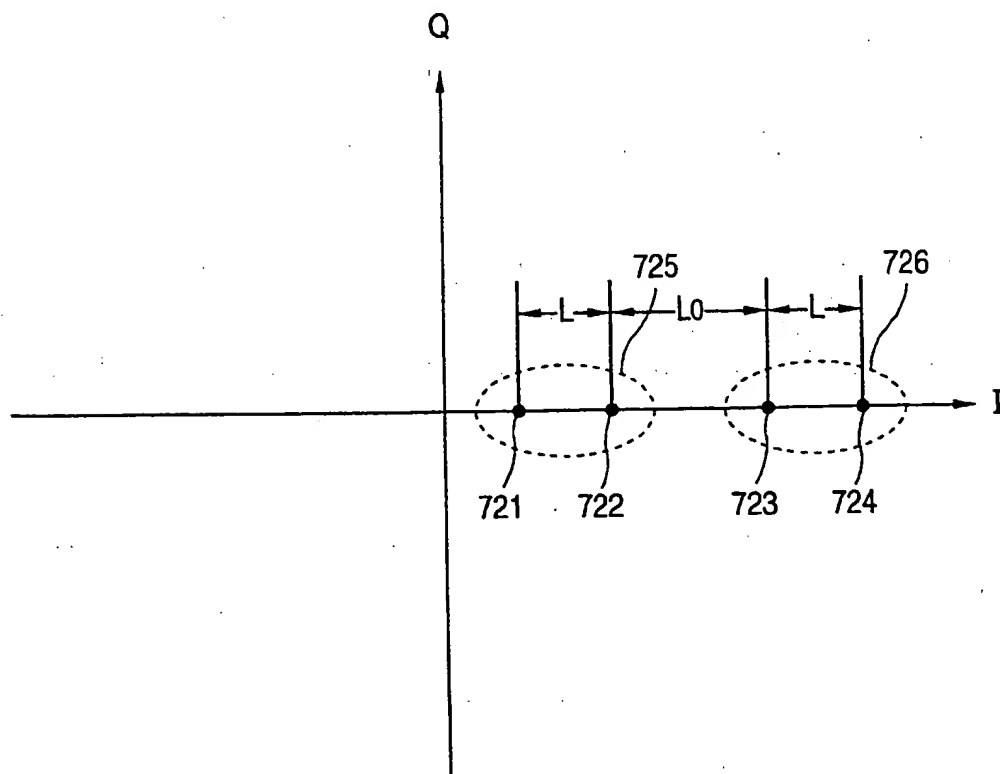
FIG. 57**FIG. 58**

FIG. 59(a)

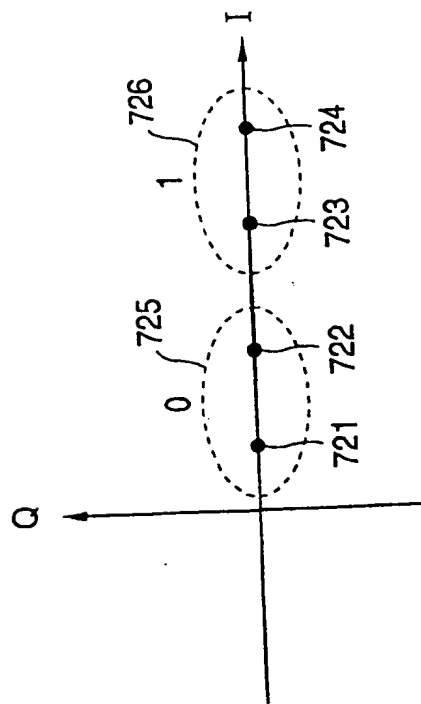


FIG. 59(c)

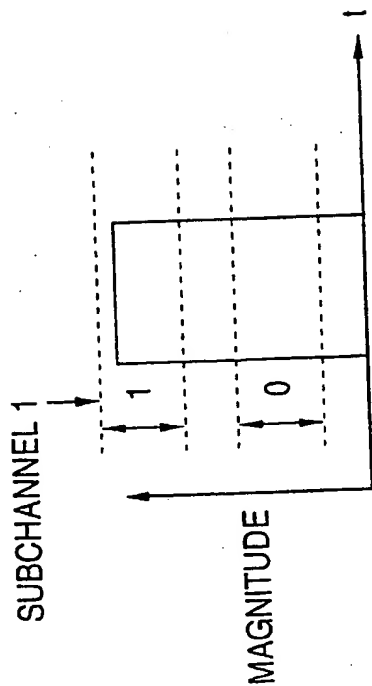


FIG. 59(b)

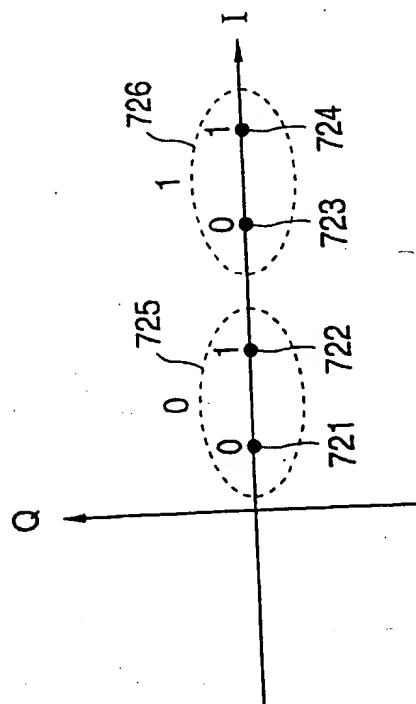


FIG. 59(d)

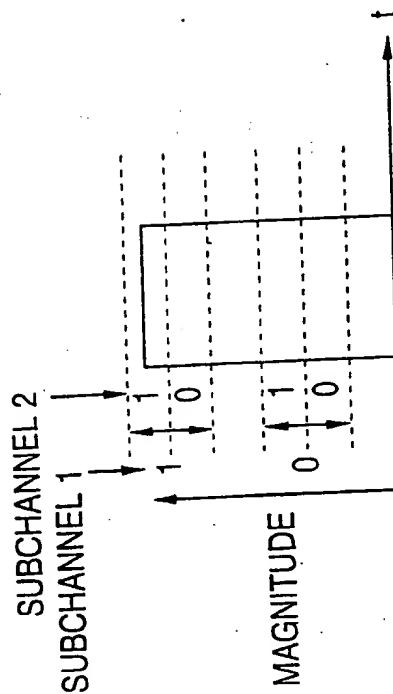


FIG. 60

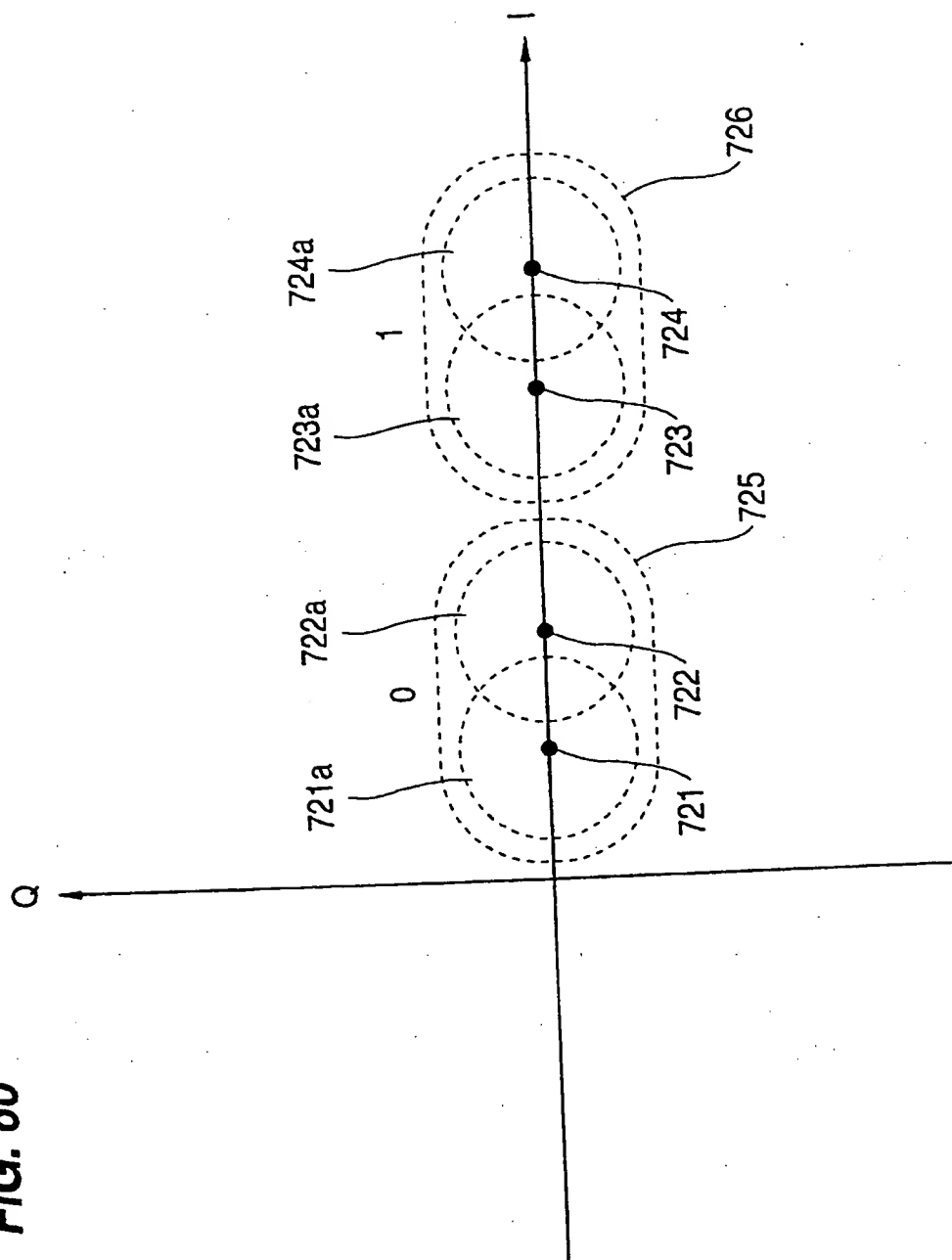


FIG. 61

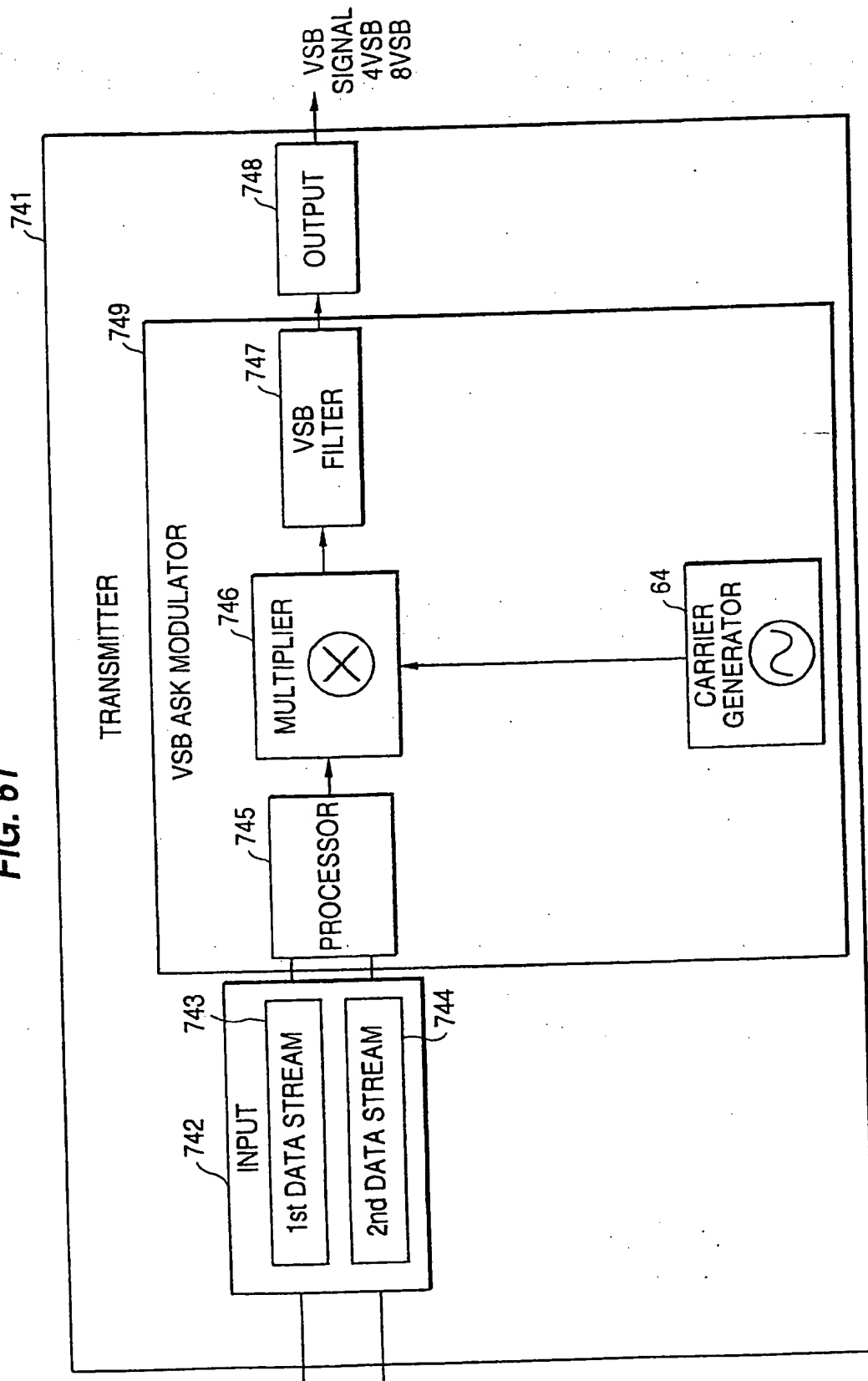


FIG. 62(a)

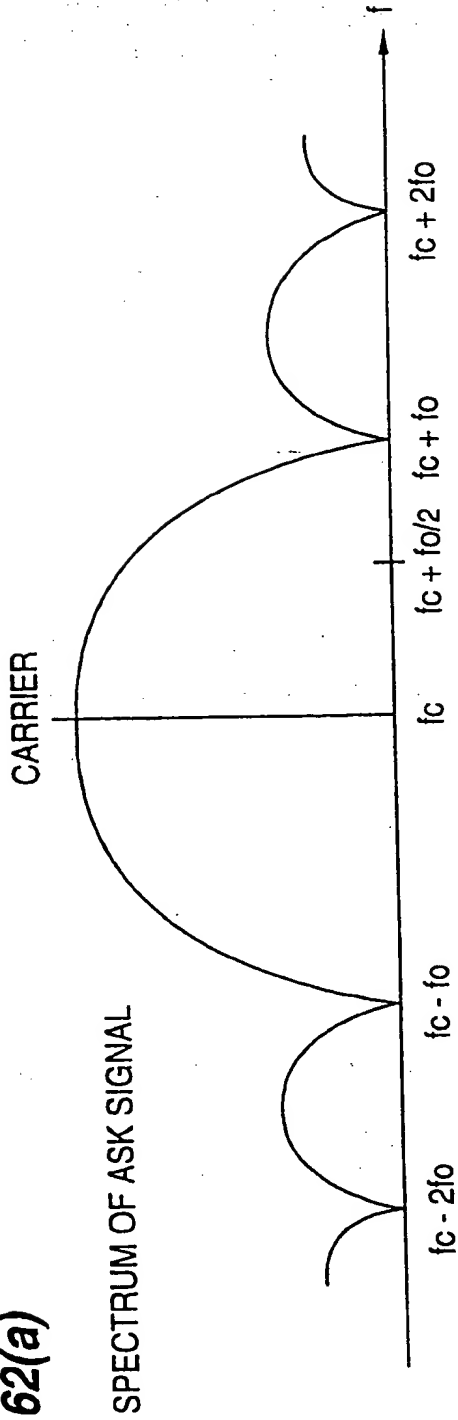


FIG. 62(b)

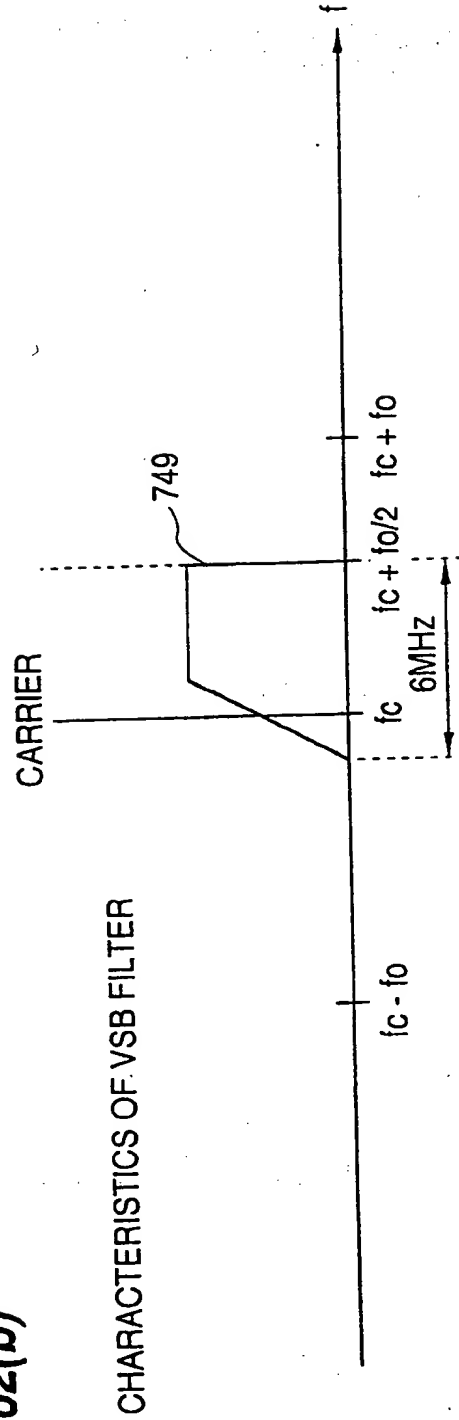


FIG. 63

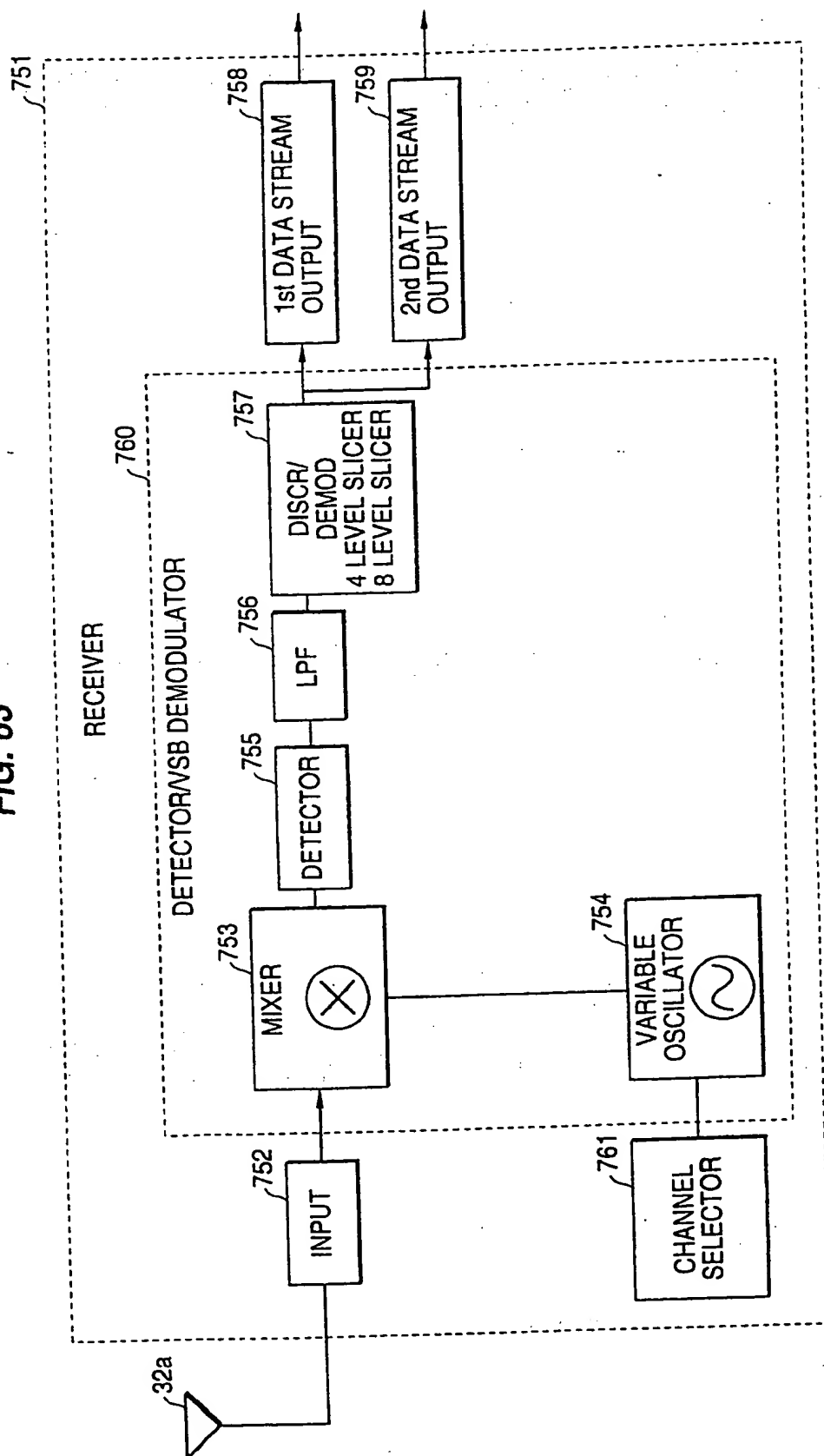


FIG. 64

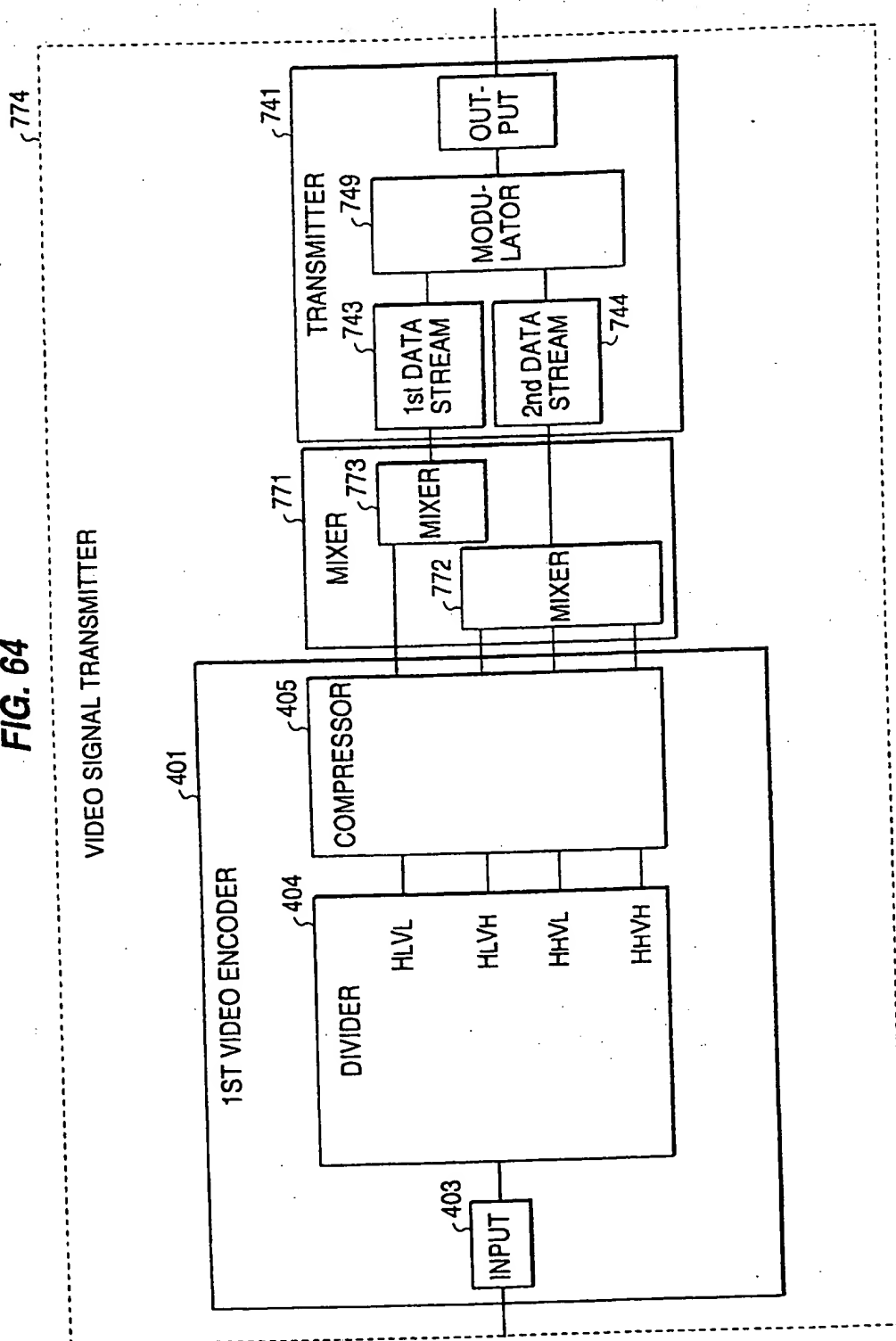


FIG. 65

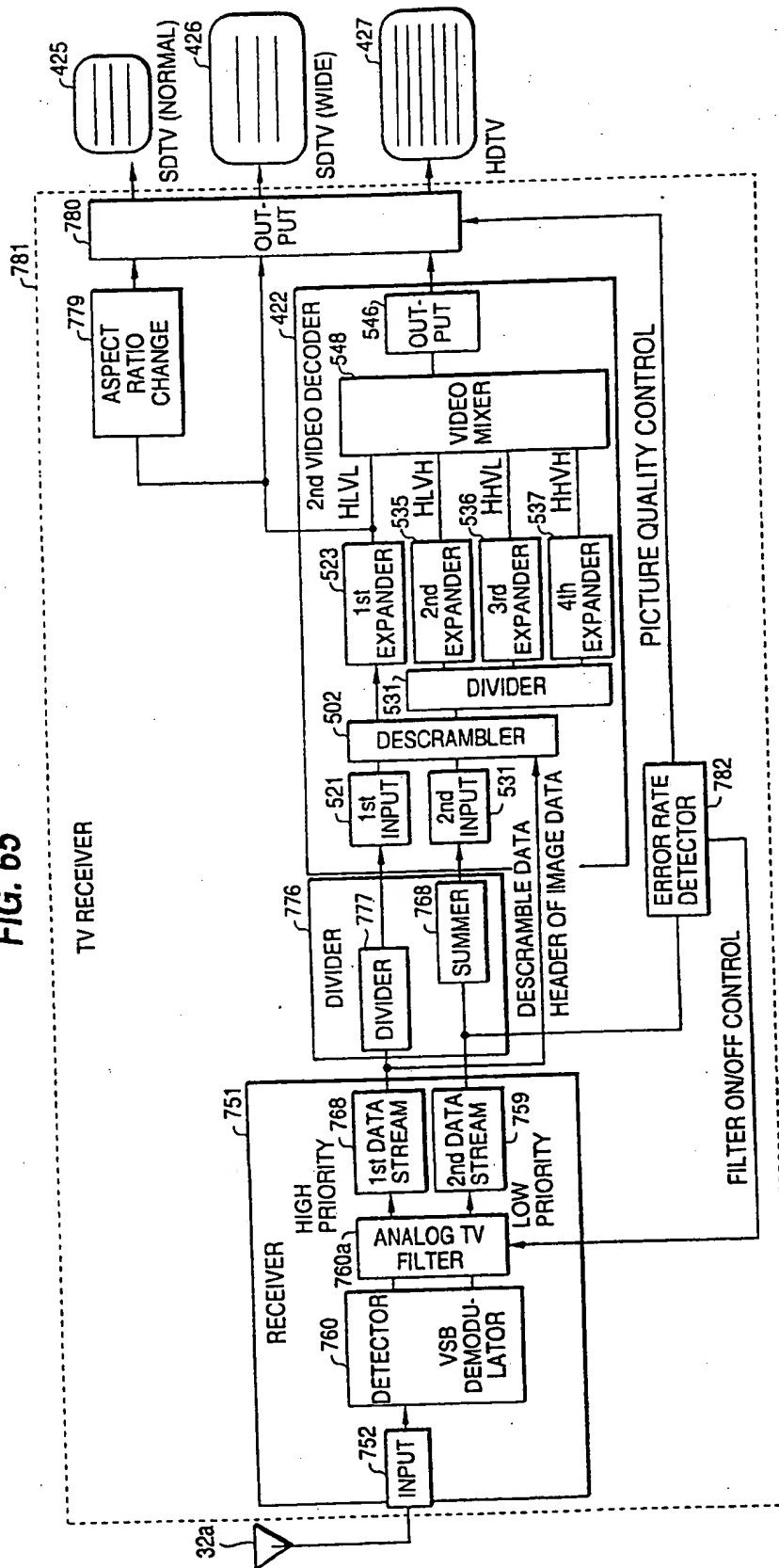
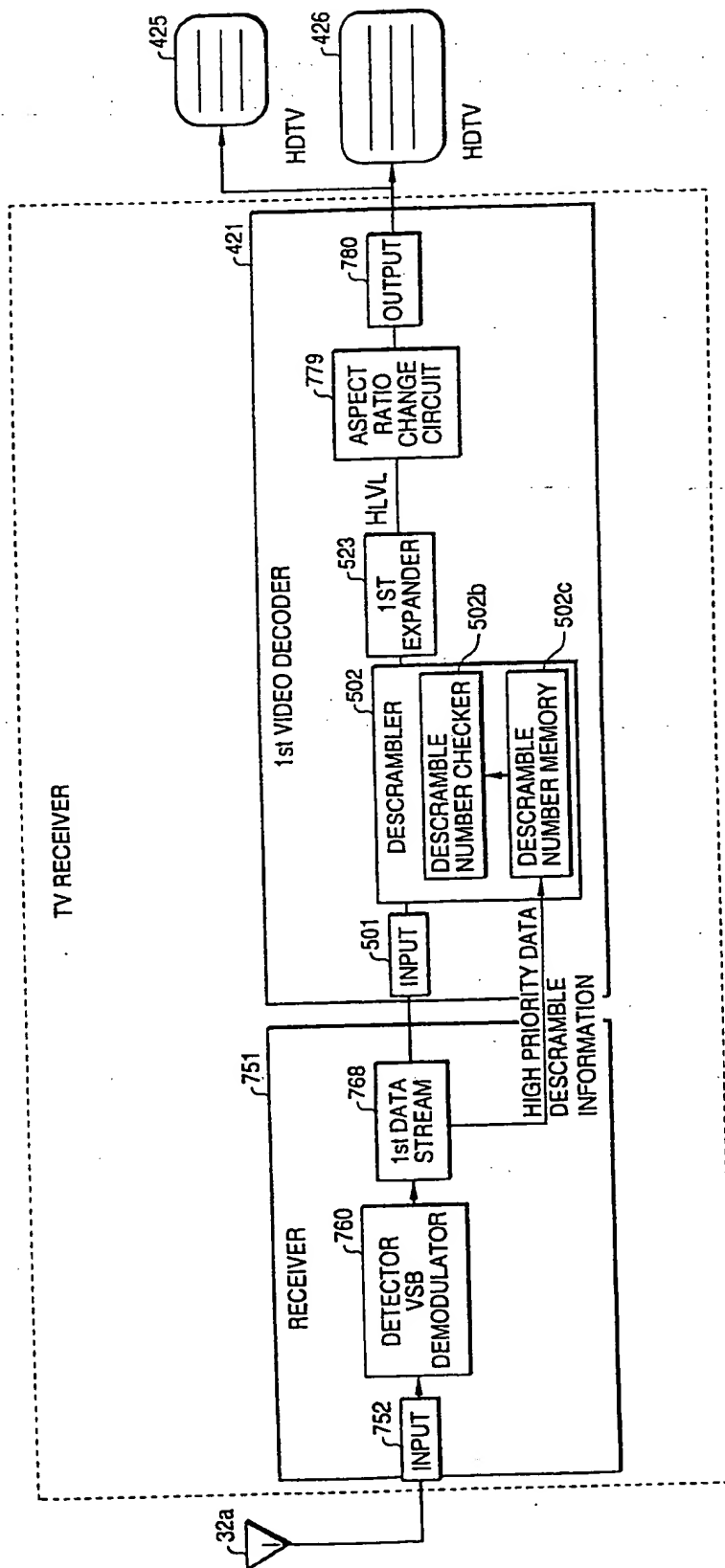
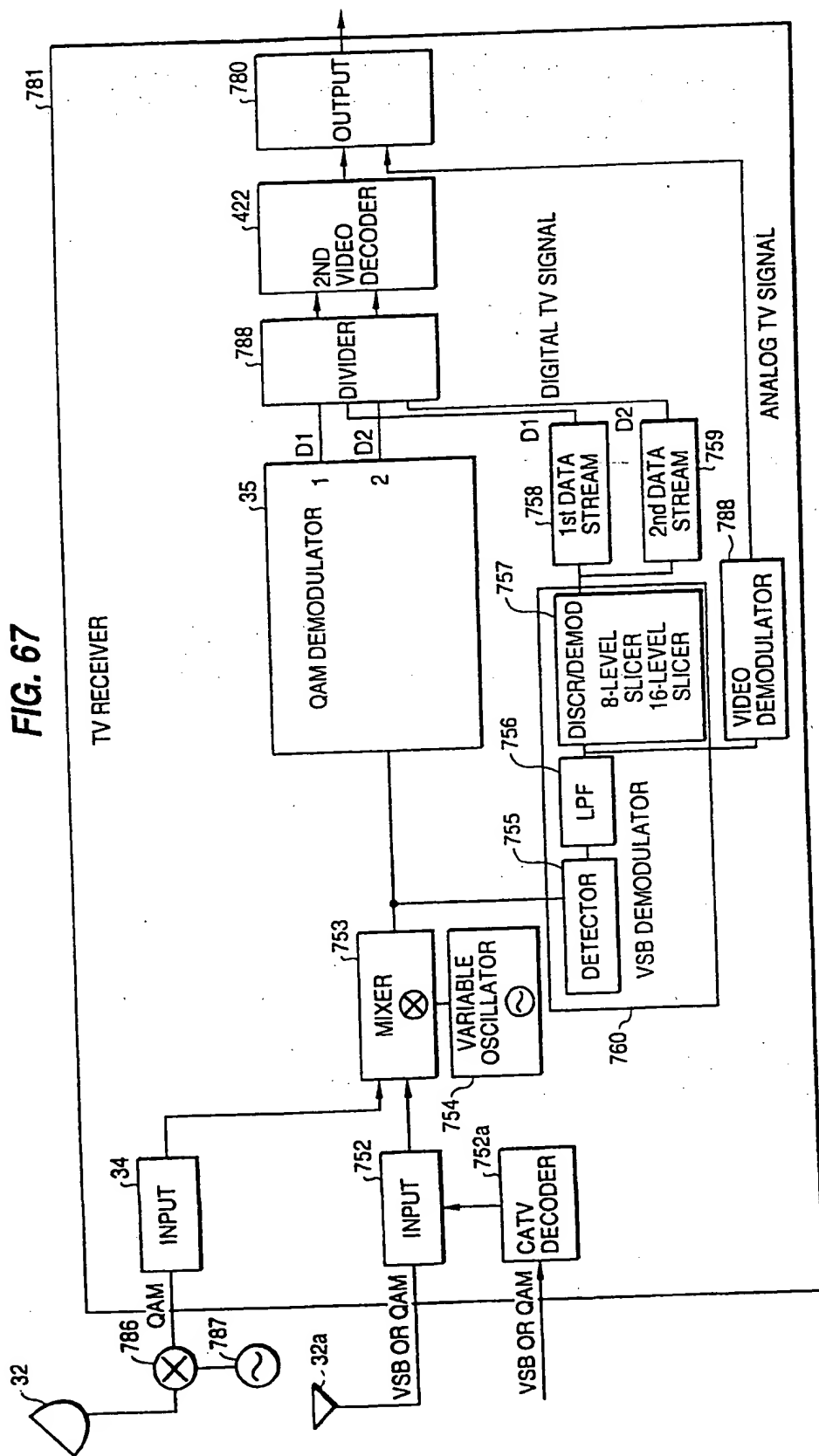


FIG. 66





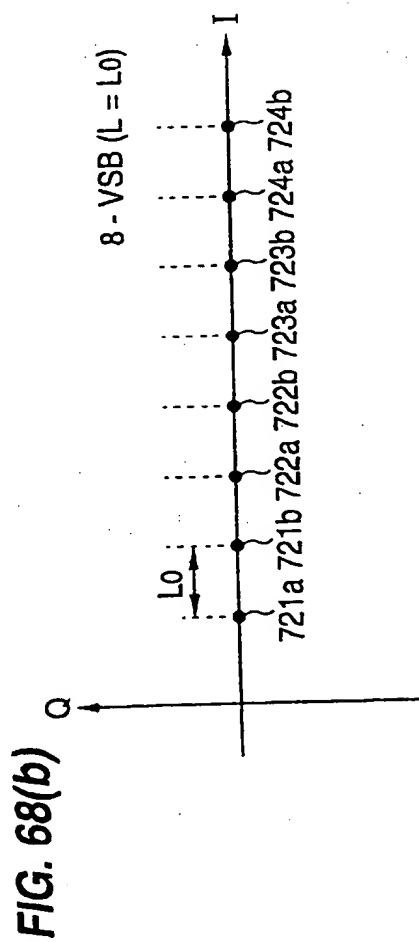
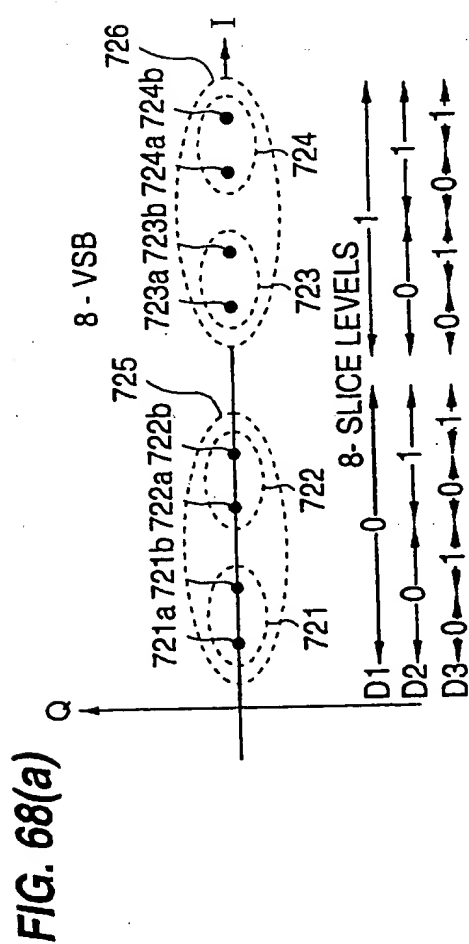


FIG. 68(c)

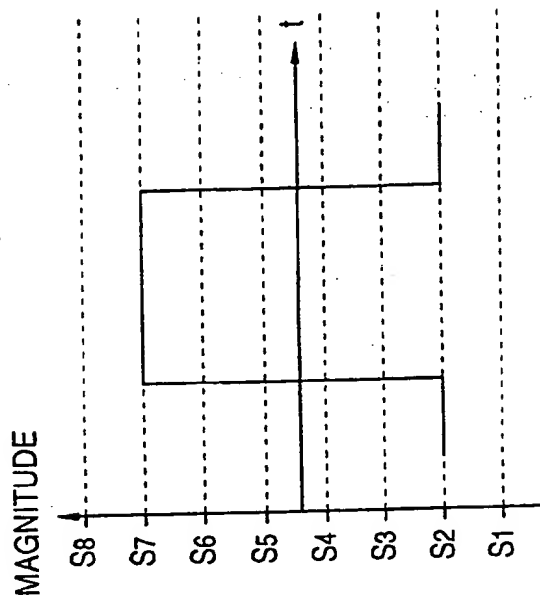


FIG. 69

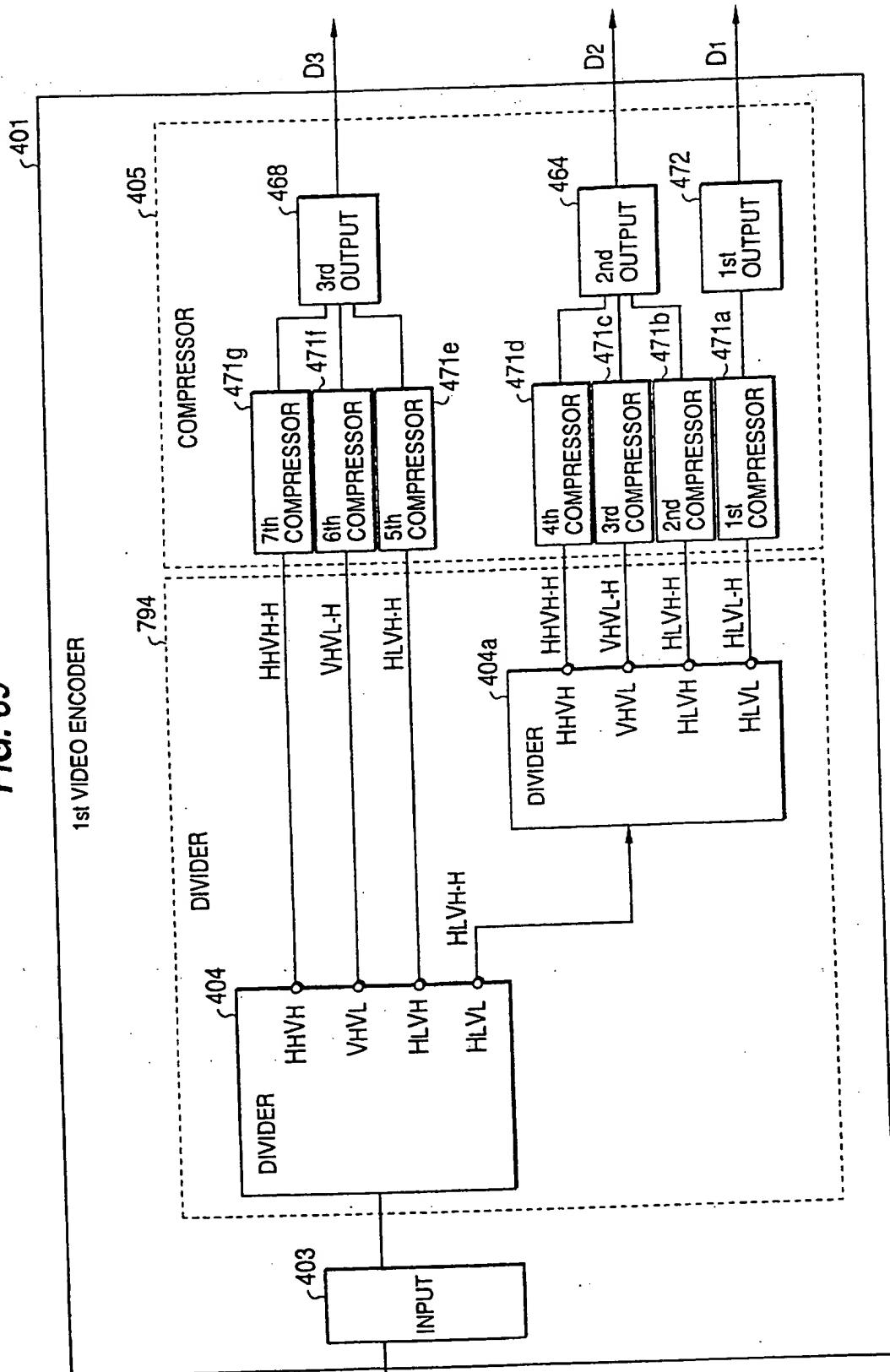


FIG. 70

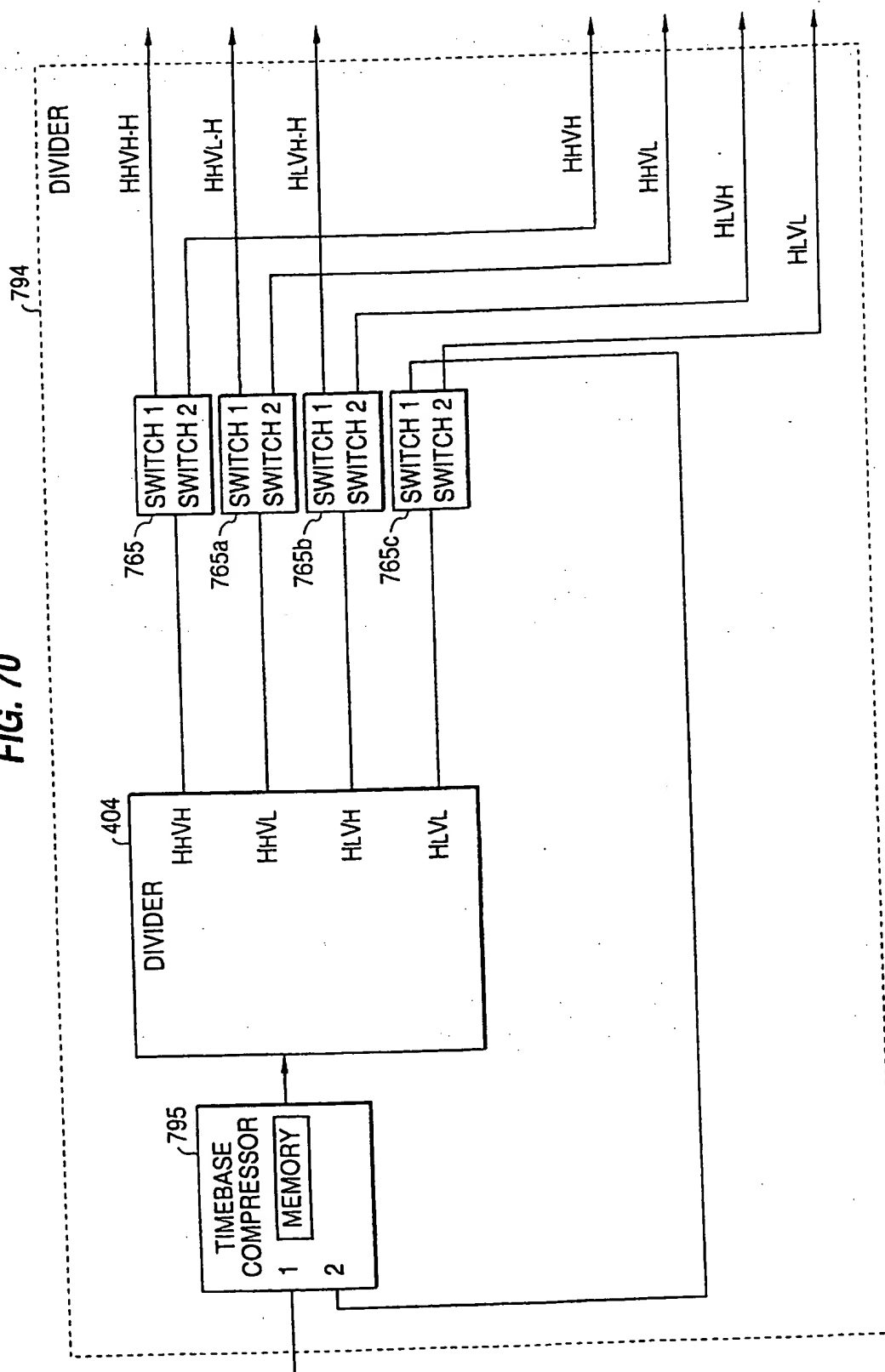


FIG. 71

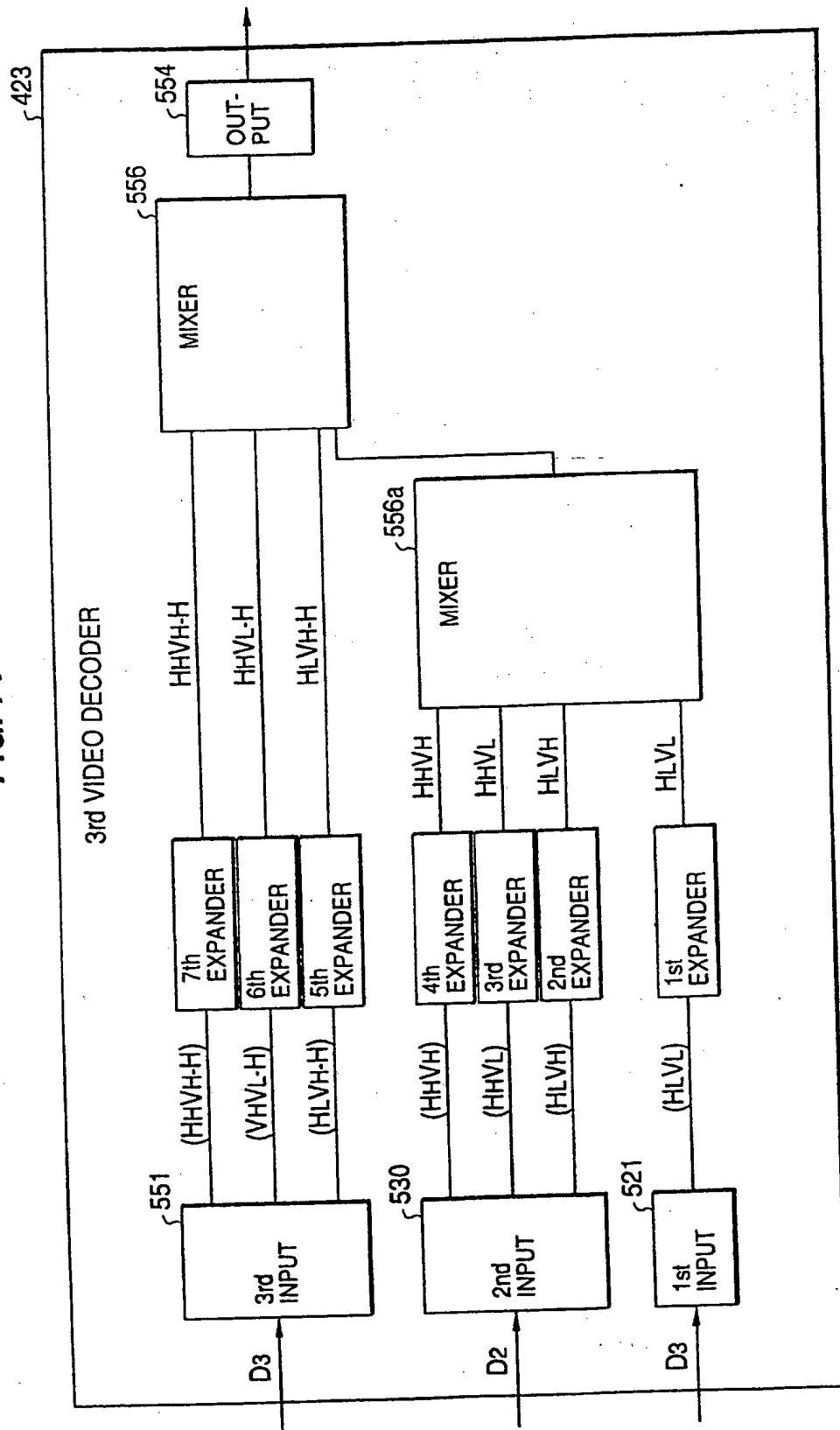


FIG. 72

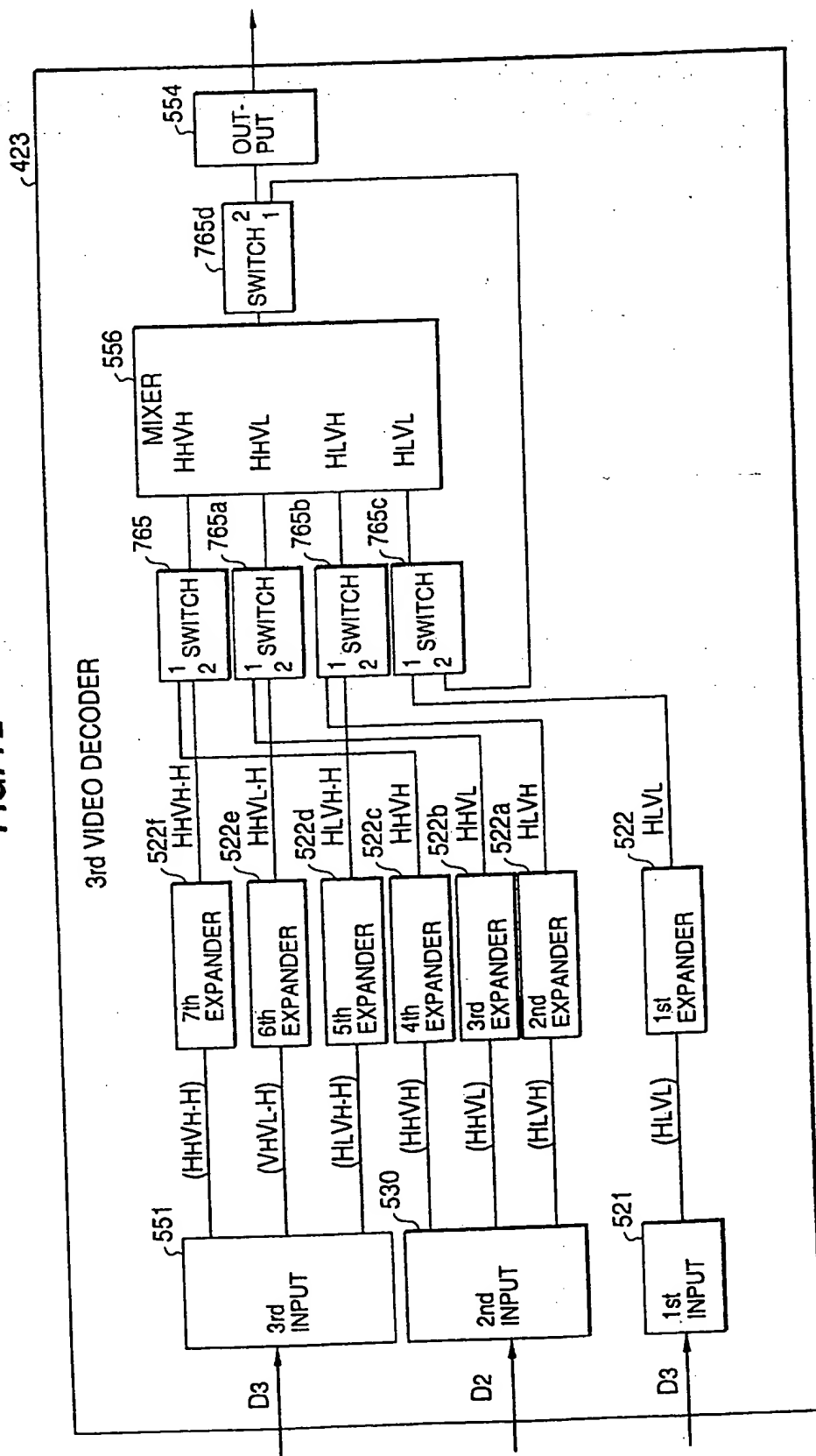


FIG. 73

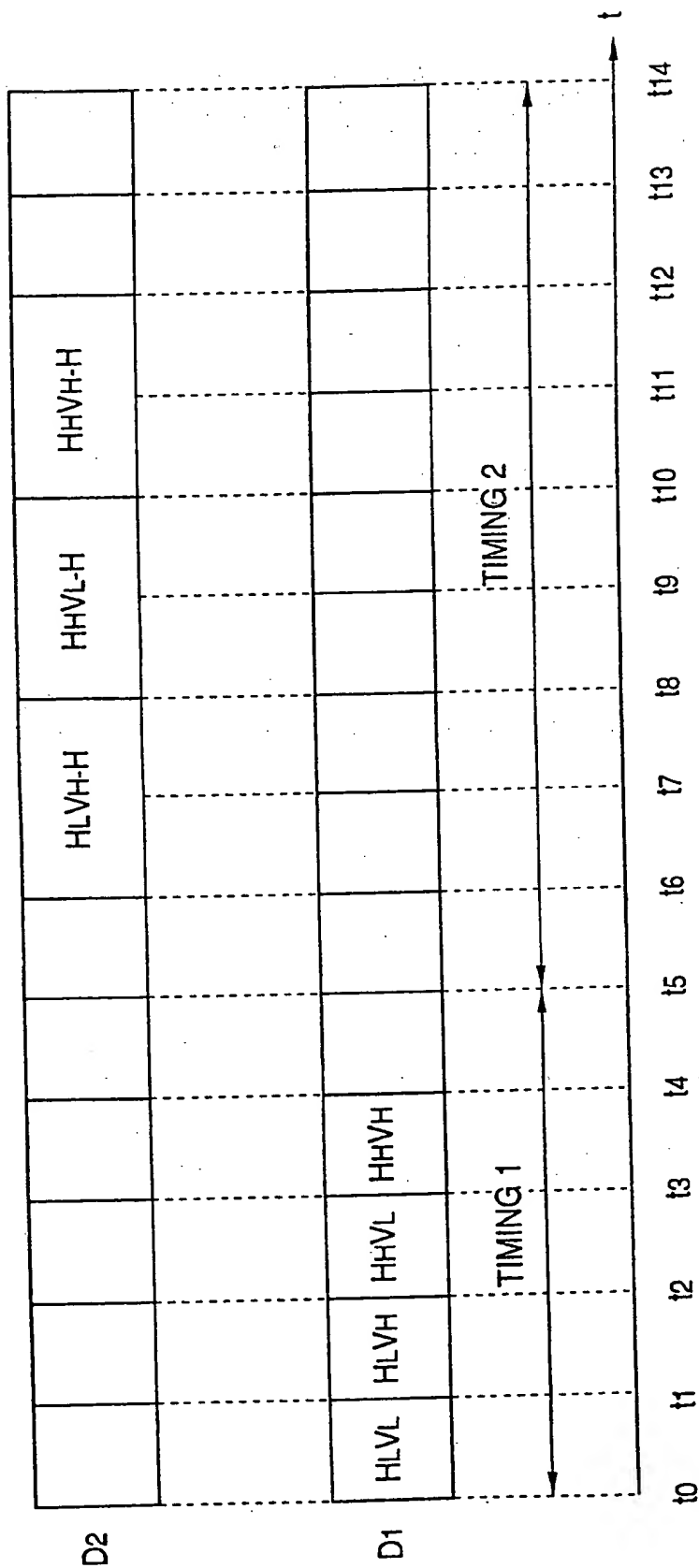


FIG. 74(a)

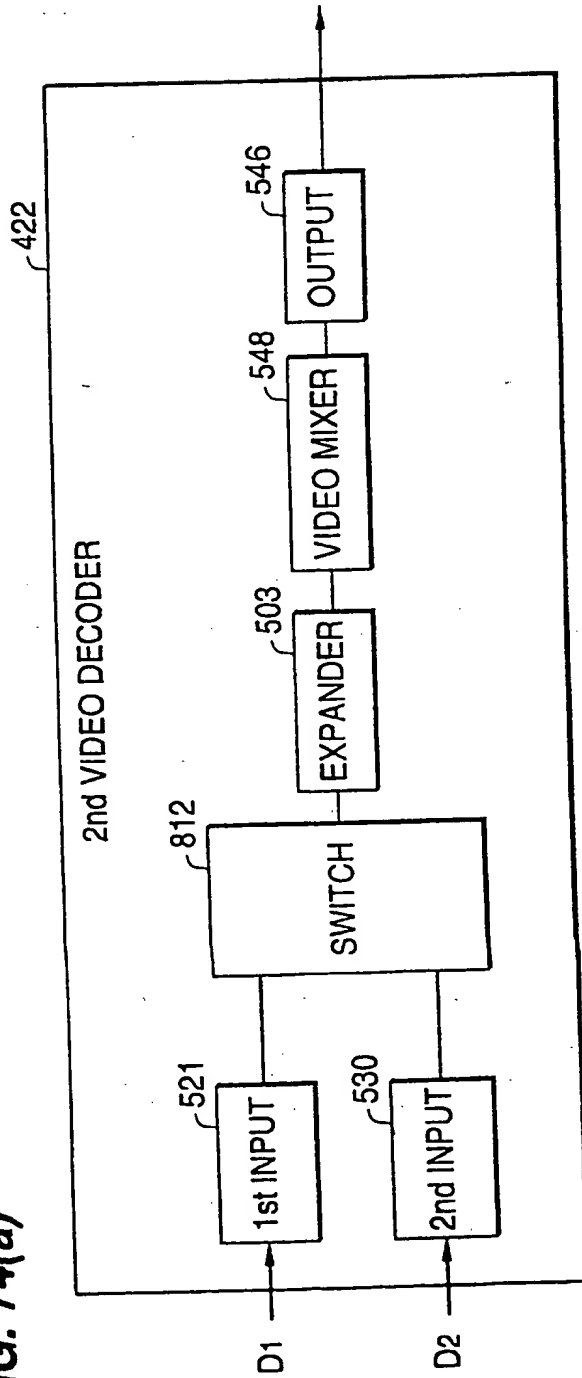


FIG. 74(b)

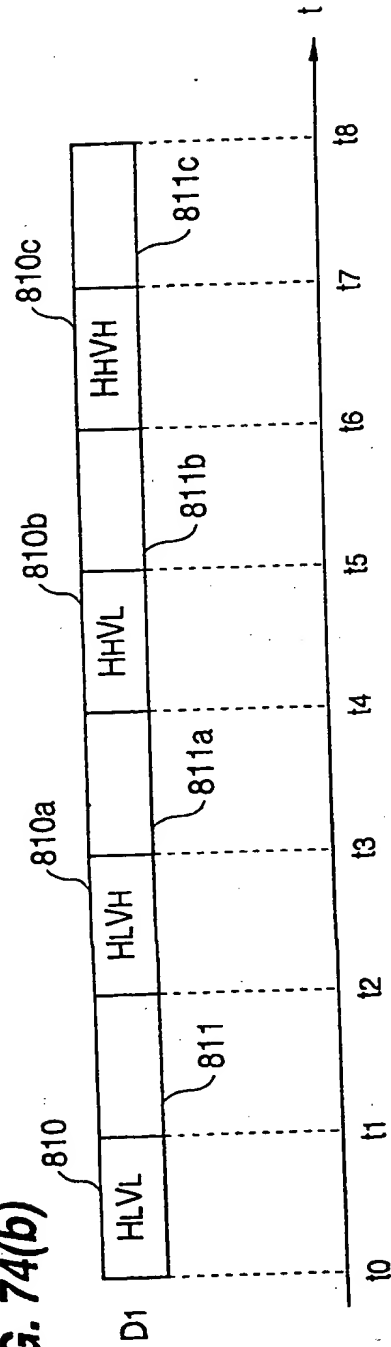


FIG. 75

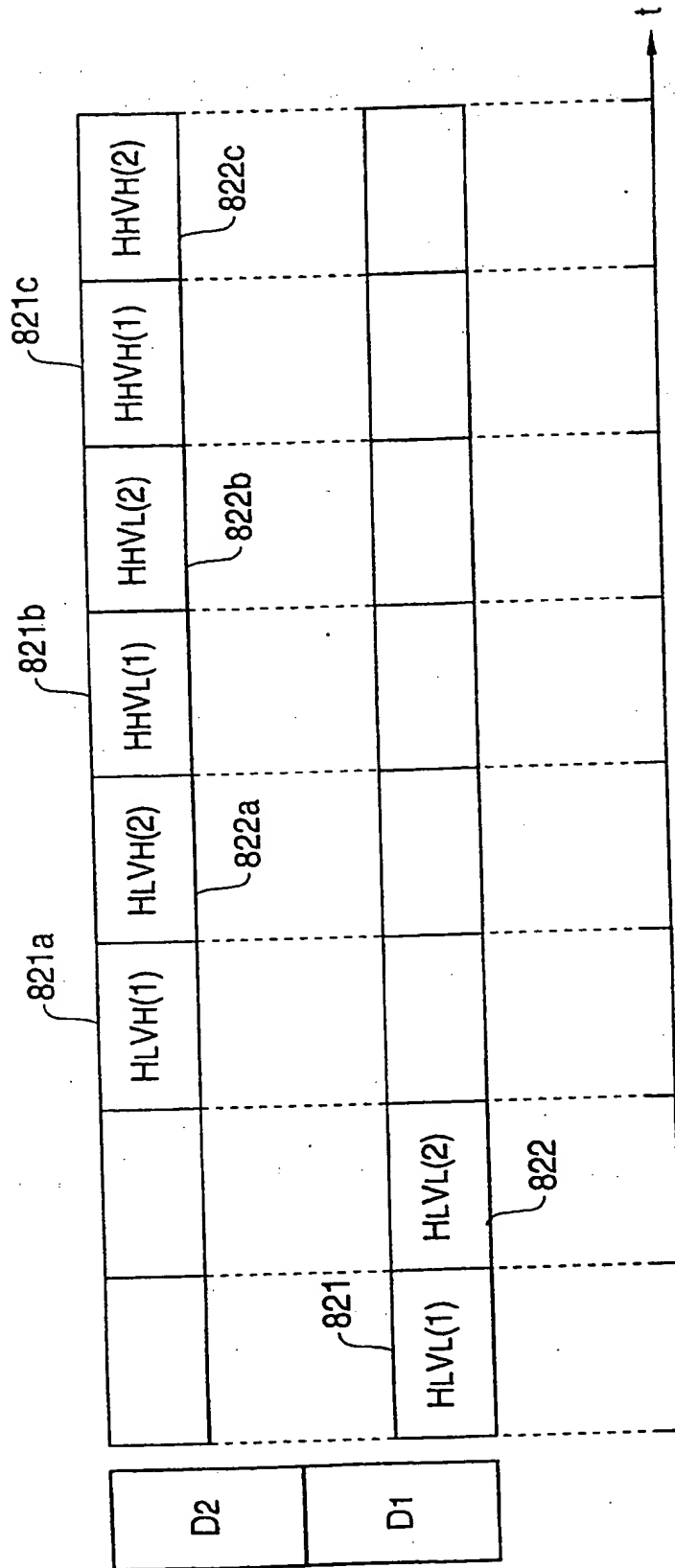


FIG. 76

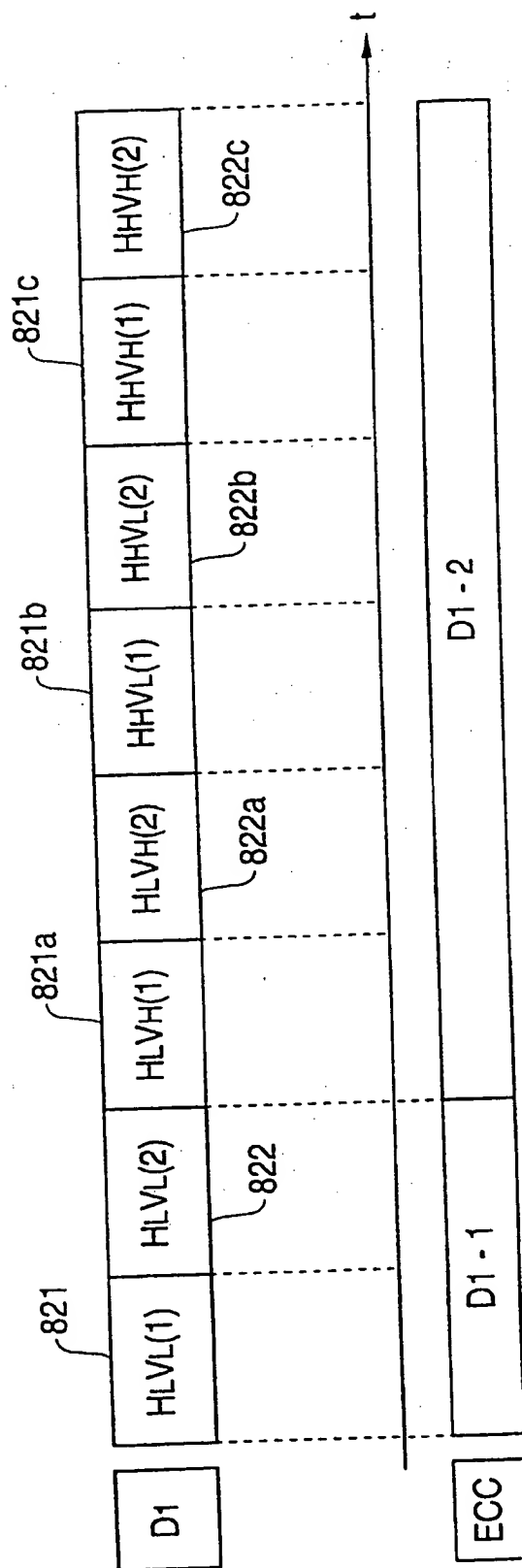


FIG. 77

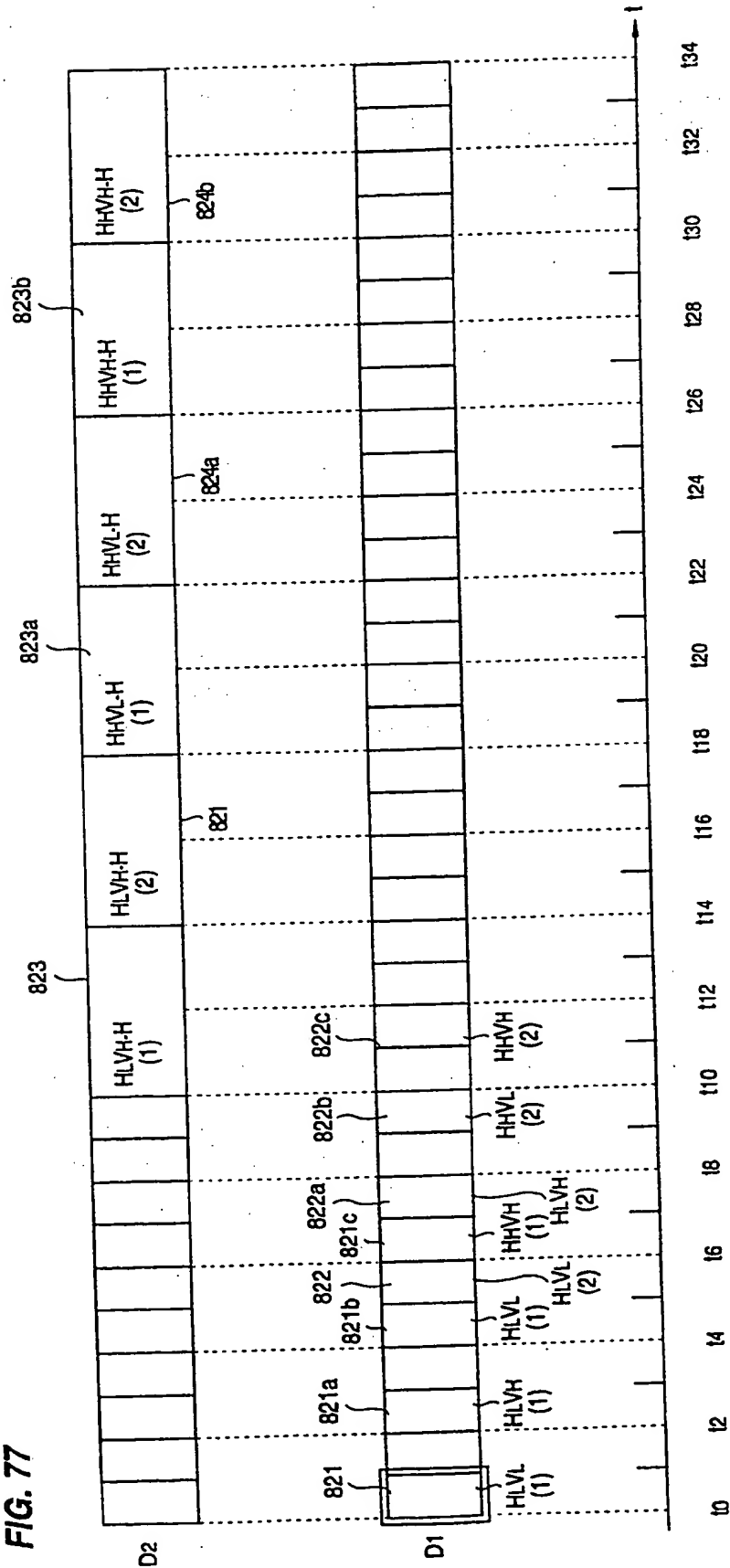


FIG. 78

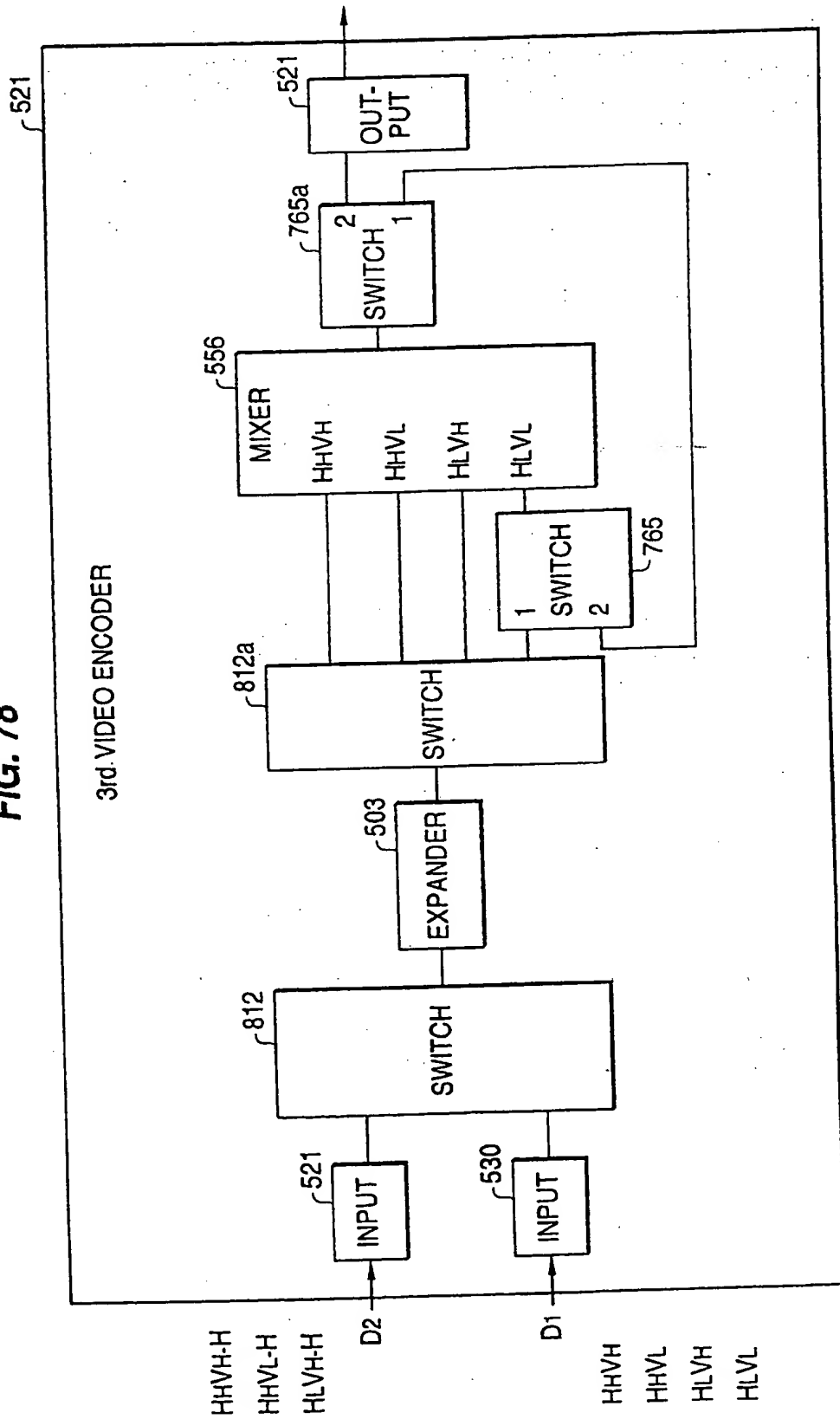


FIG. 79

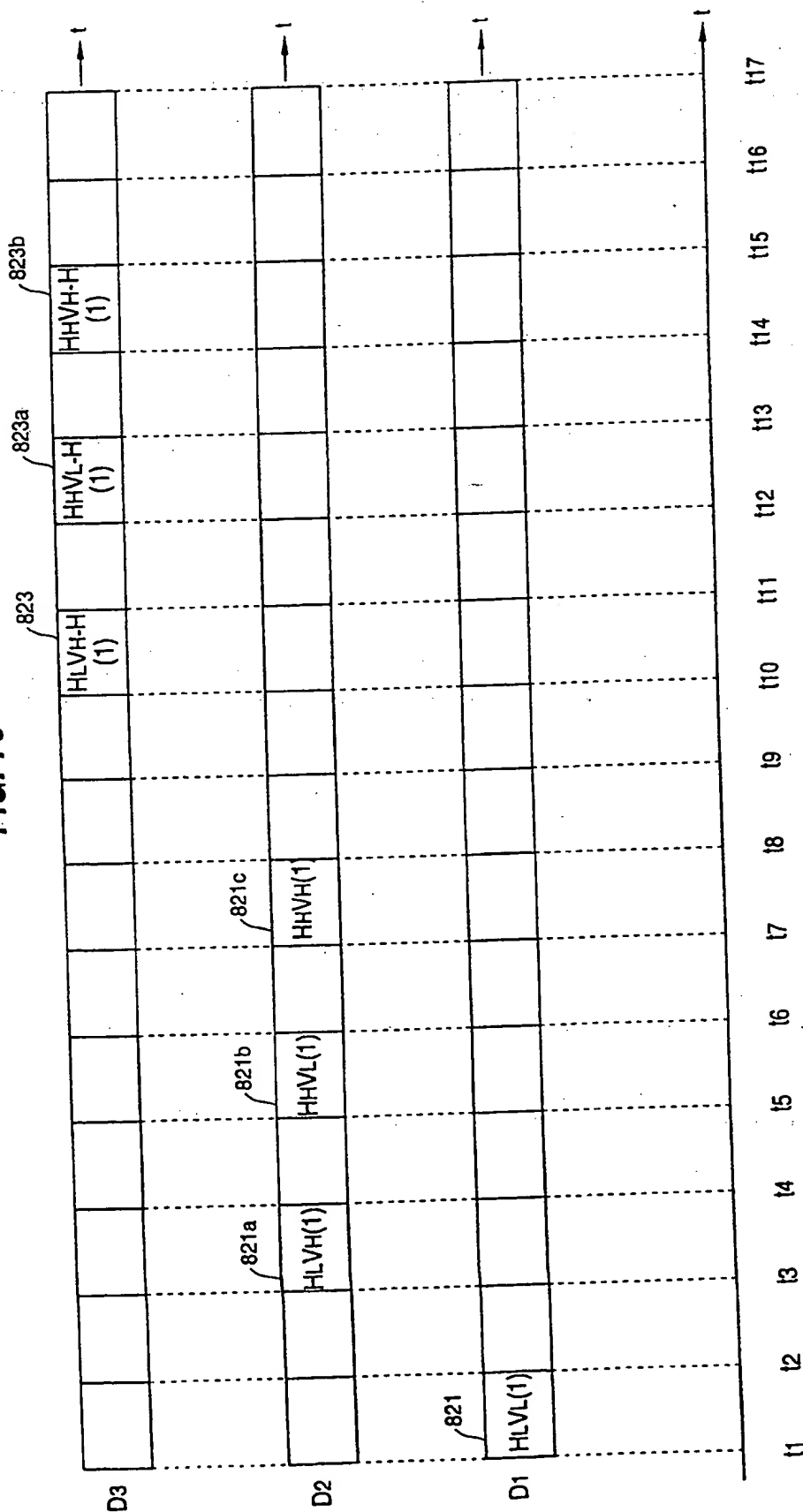


FIG. 80

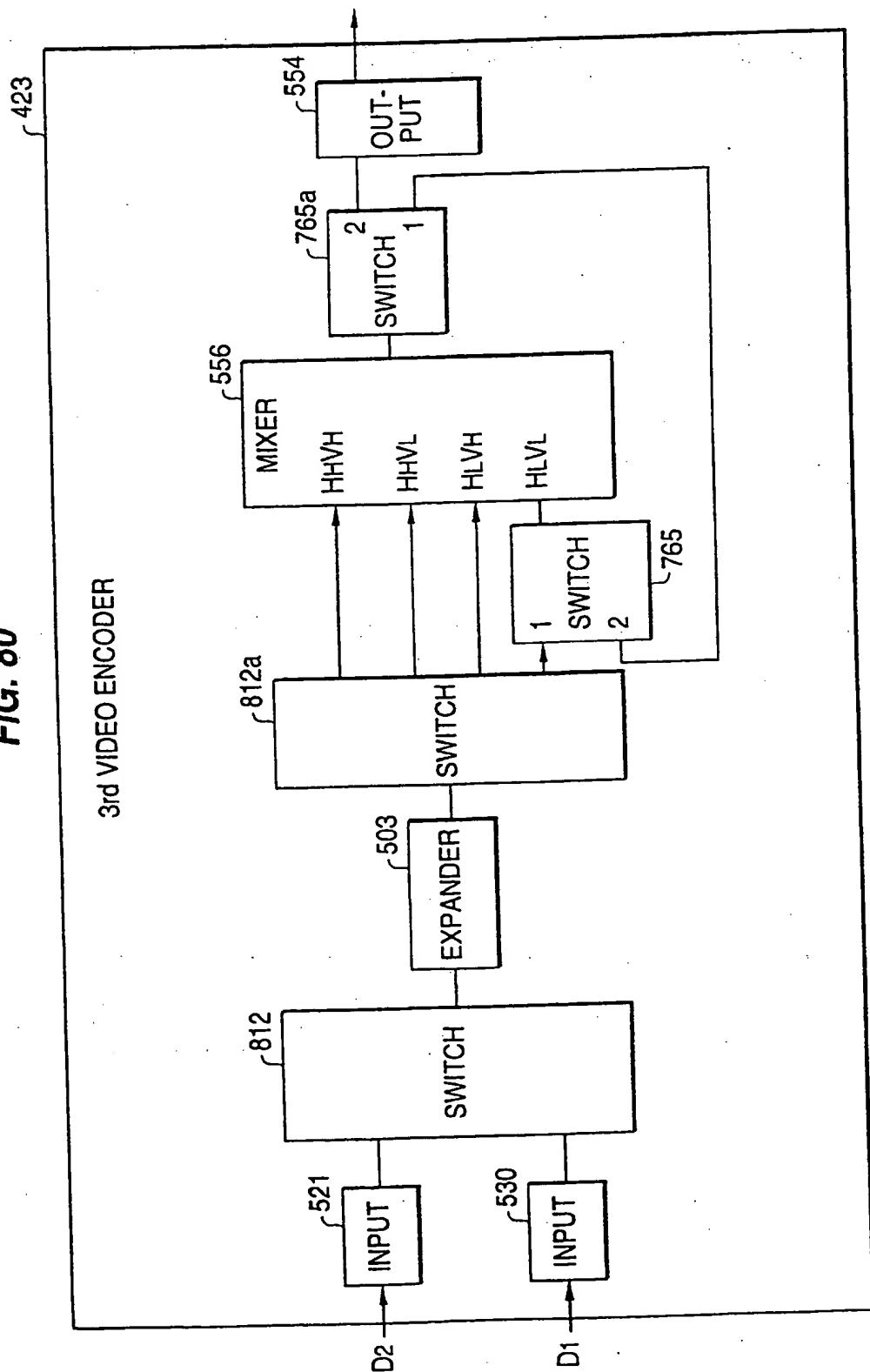


FIG. 81

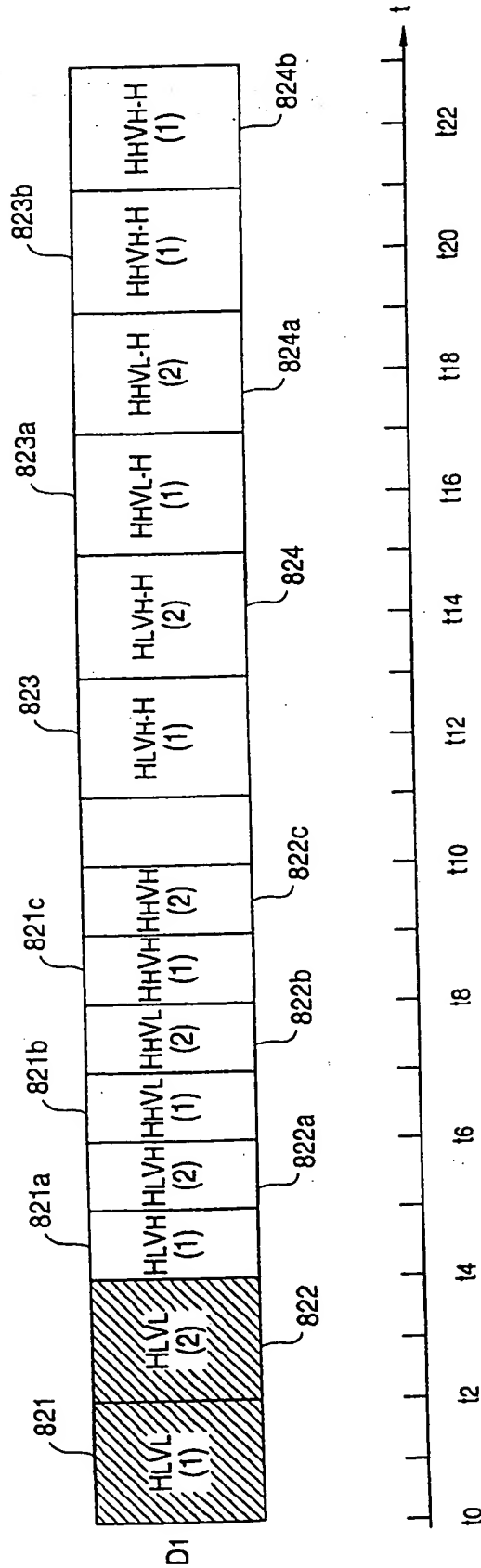


FIG. 82

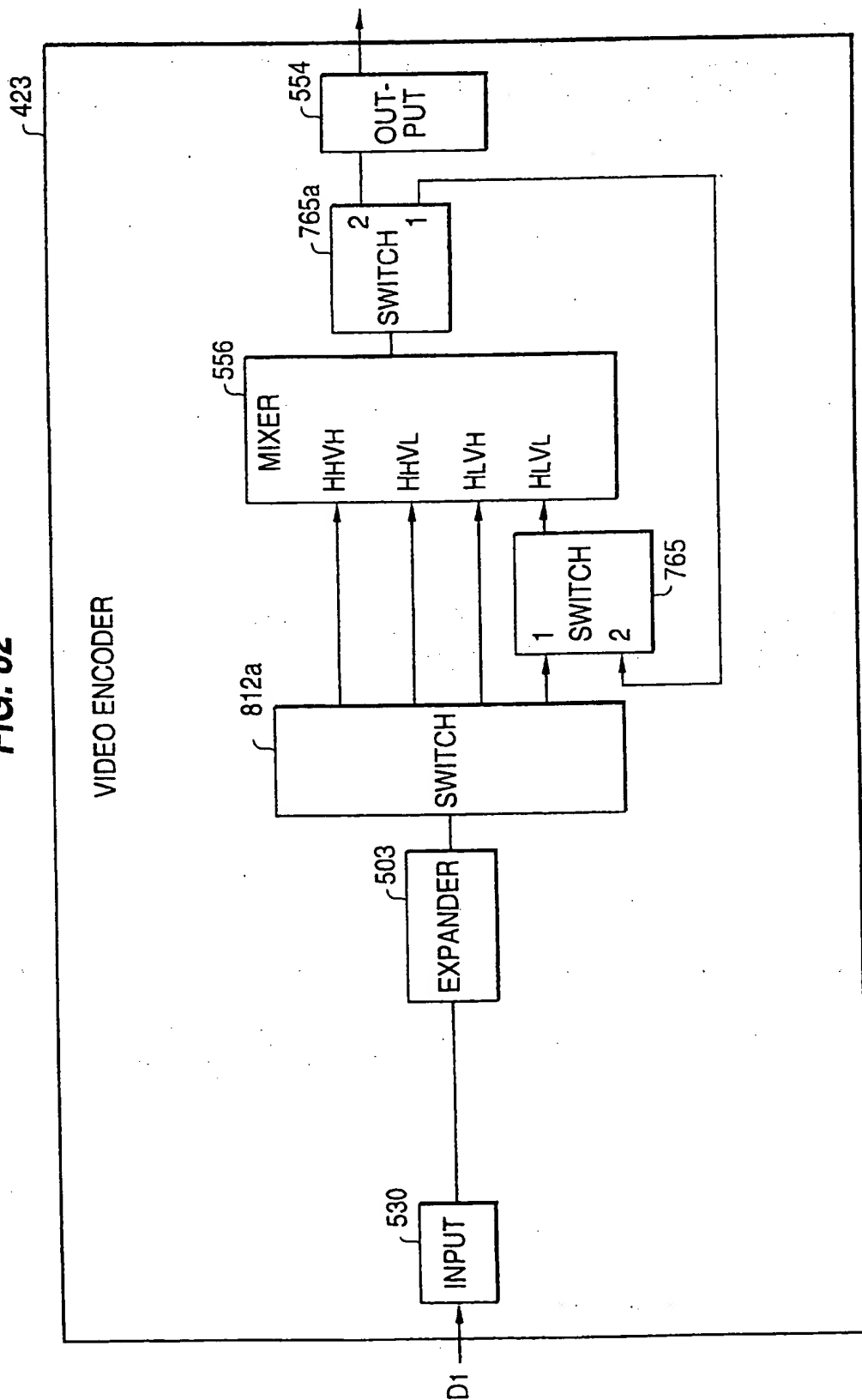


FIG. 83

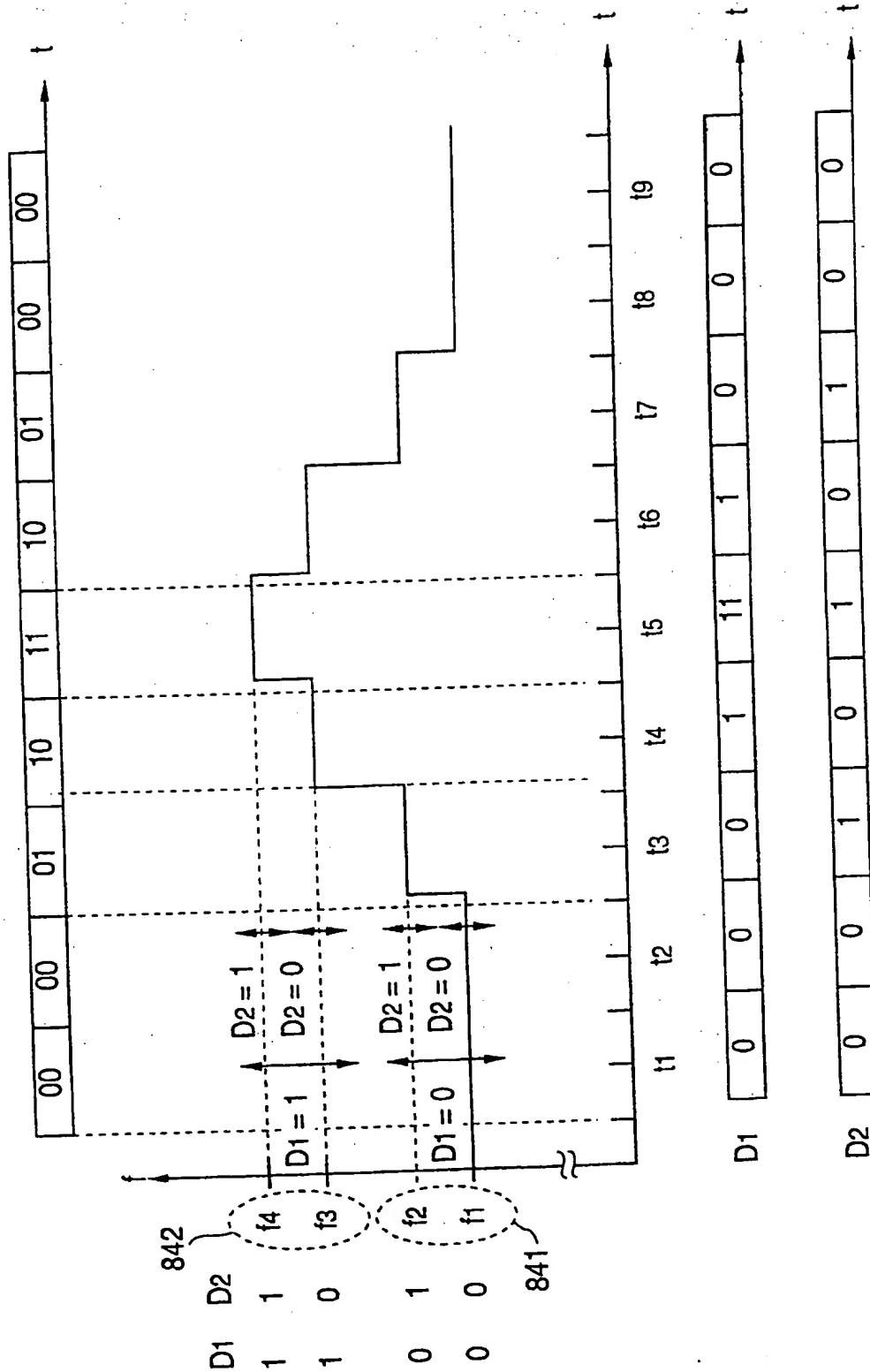


FIG. 84

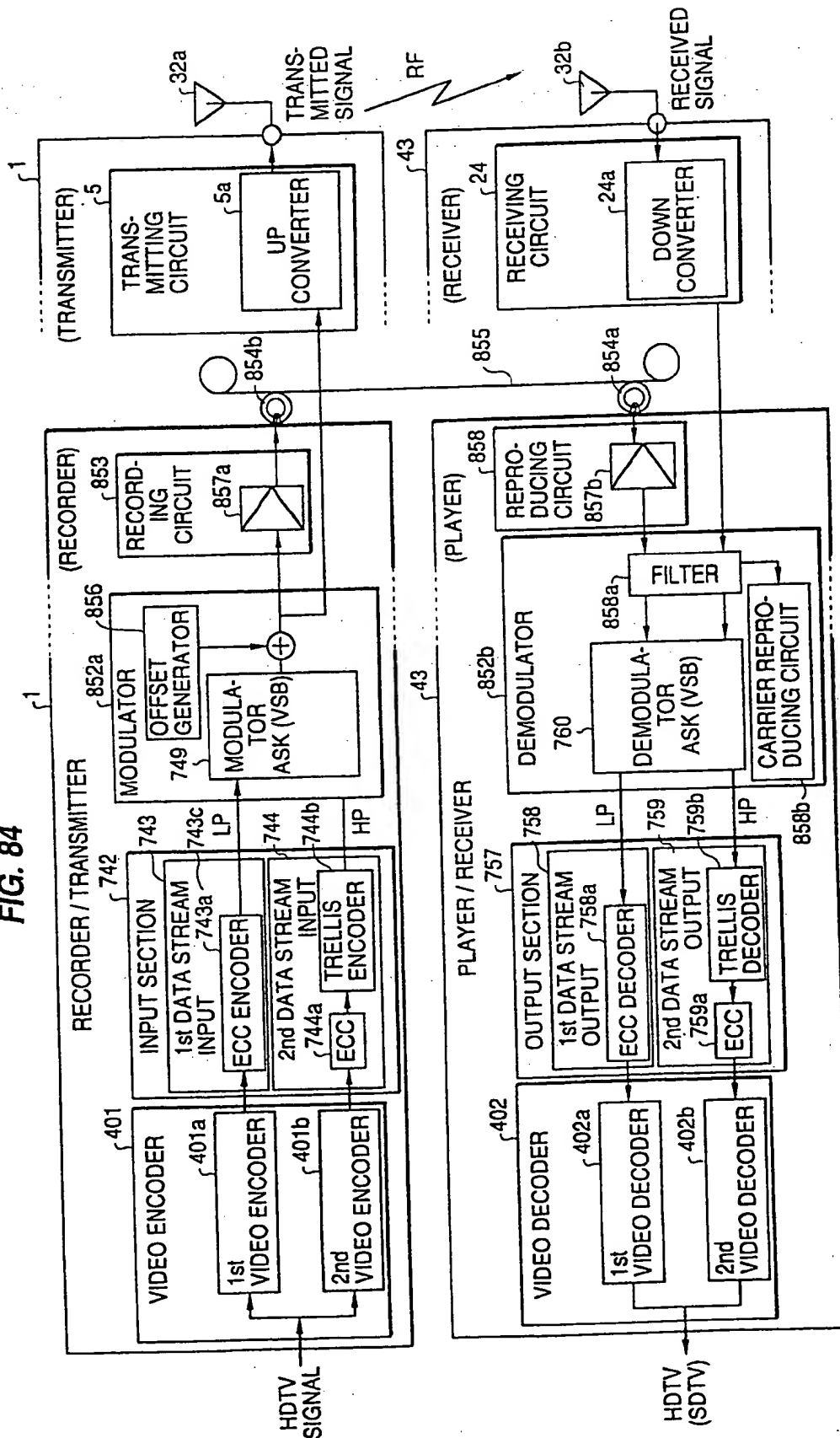


FIG. 85

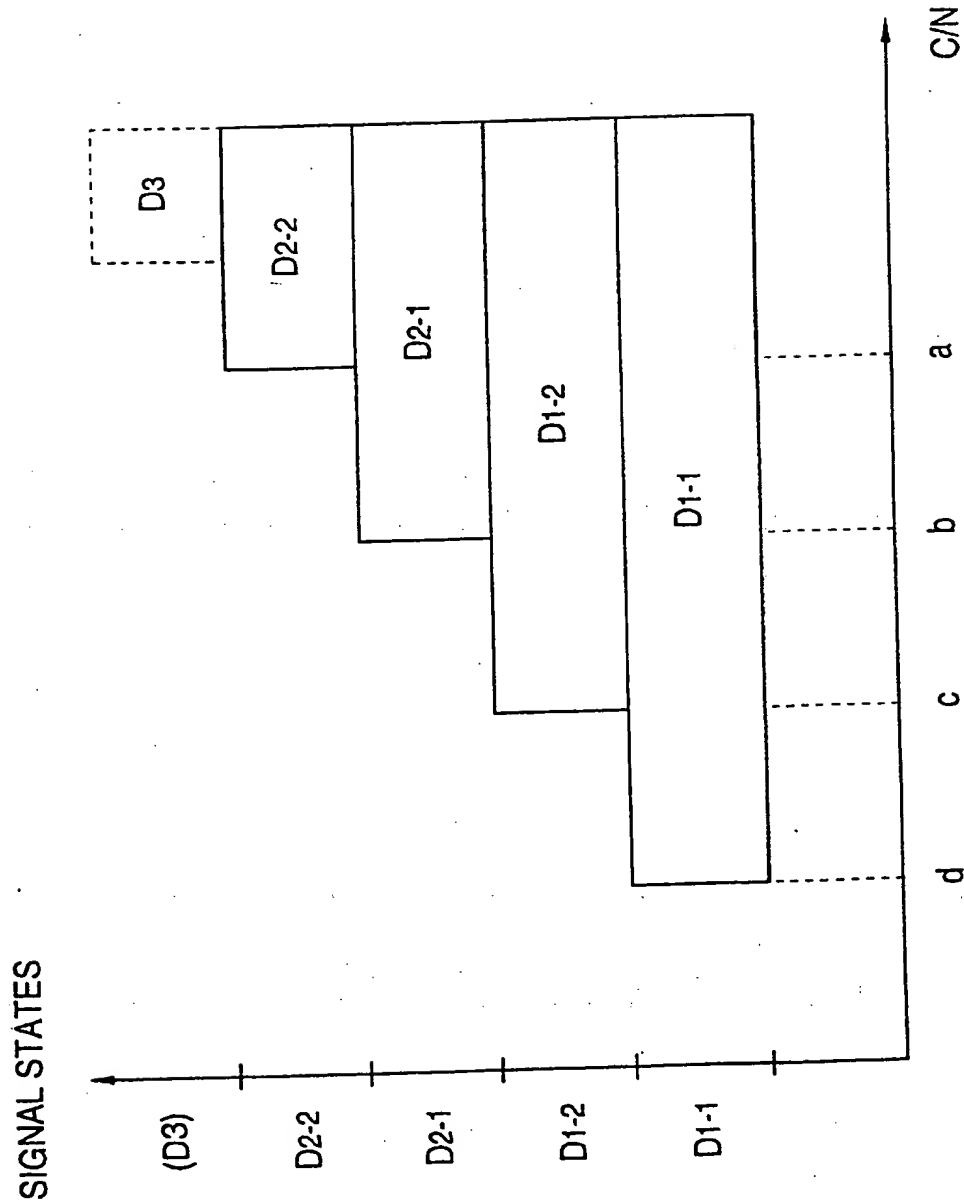


FIG. 86

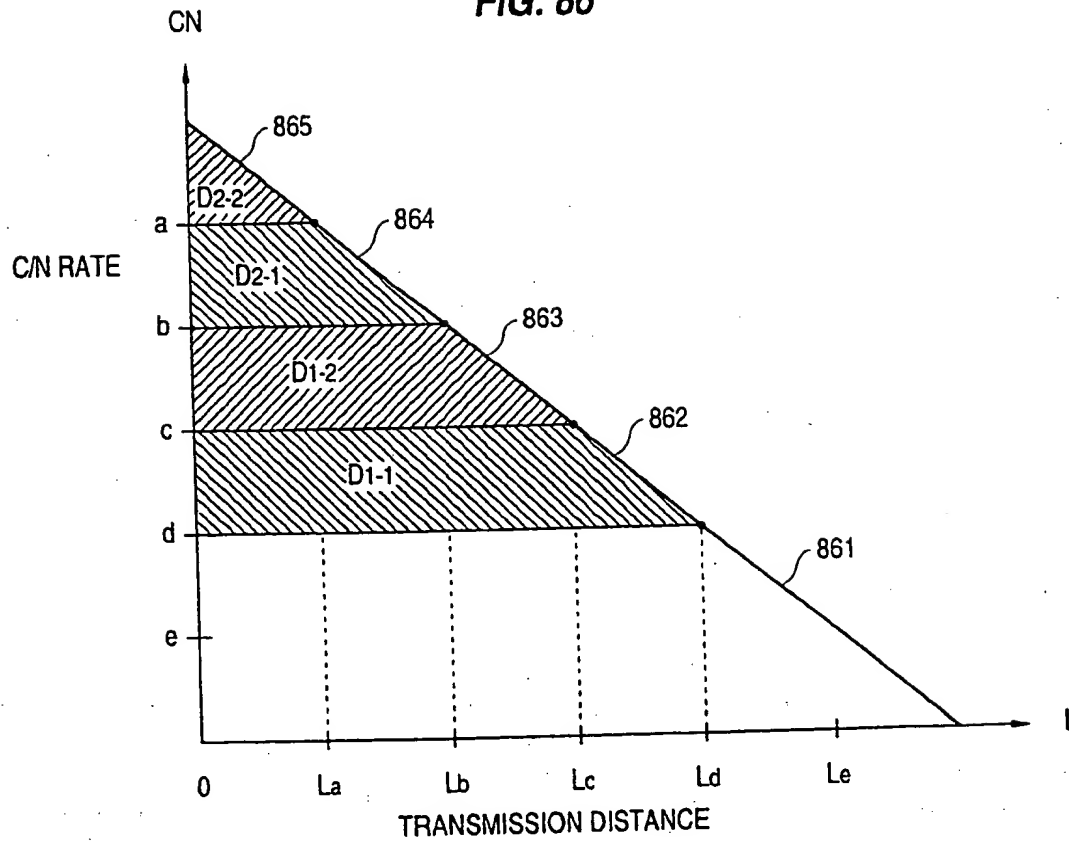


FIG. 87

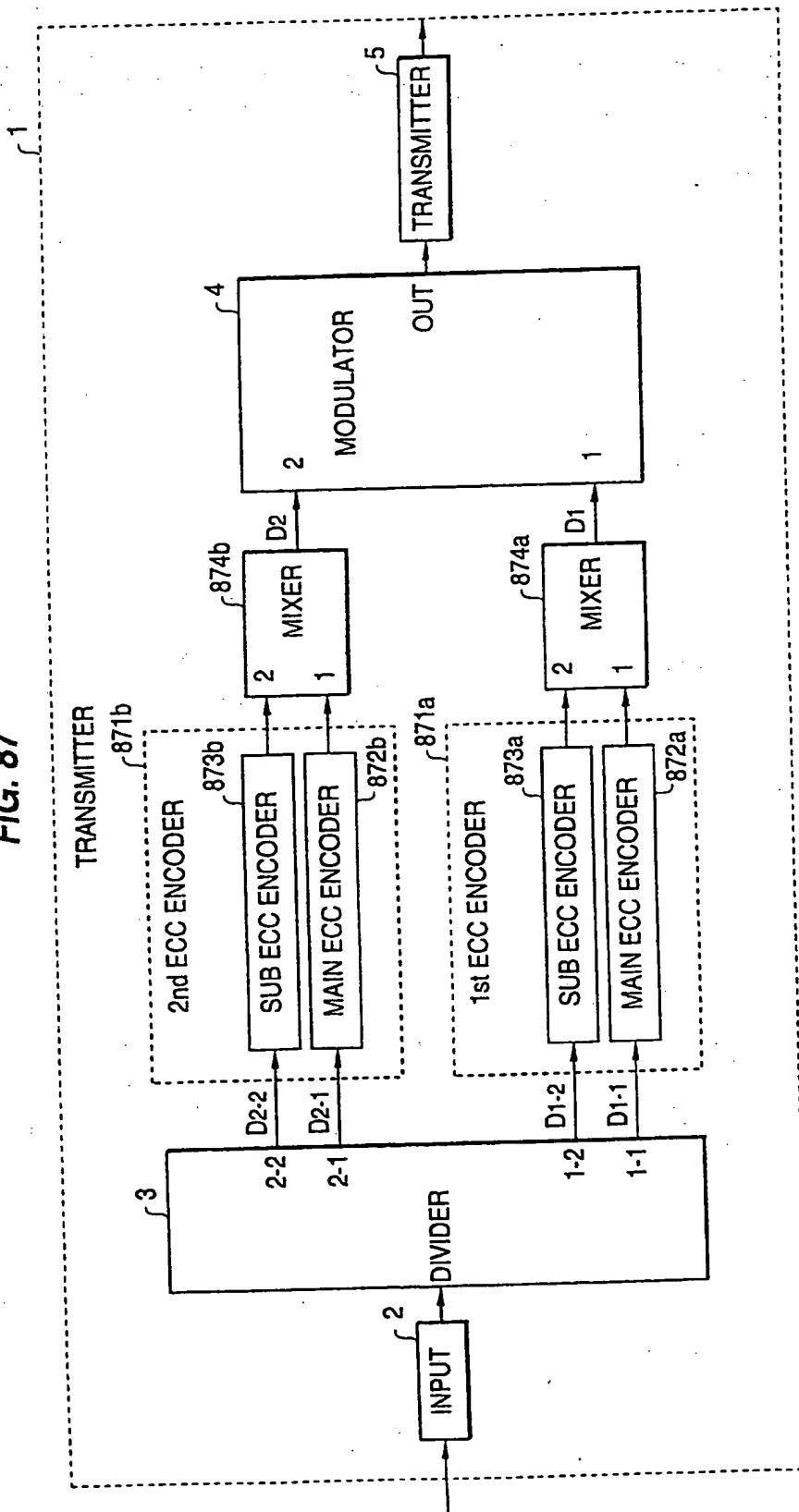


FIG. 88

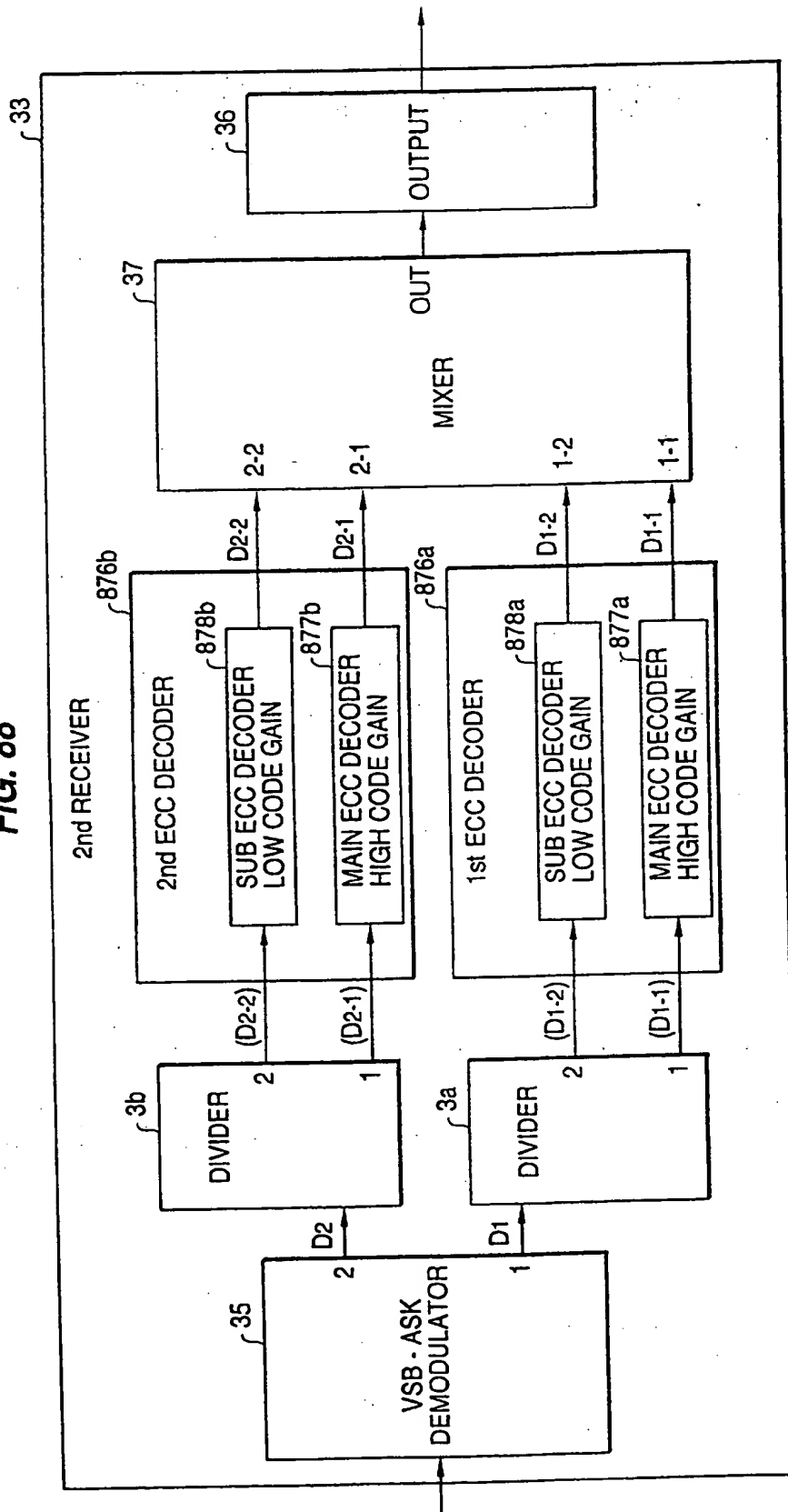


FIG. 89

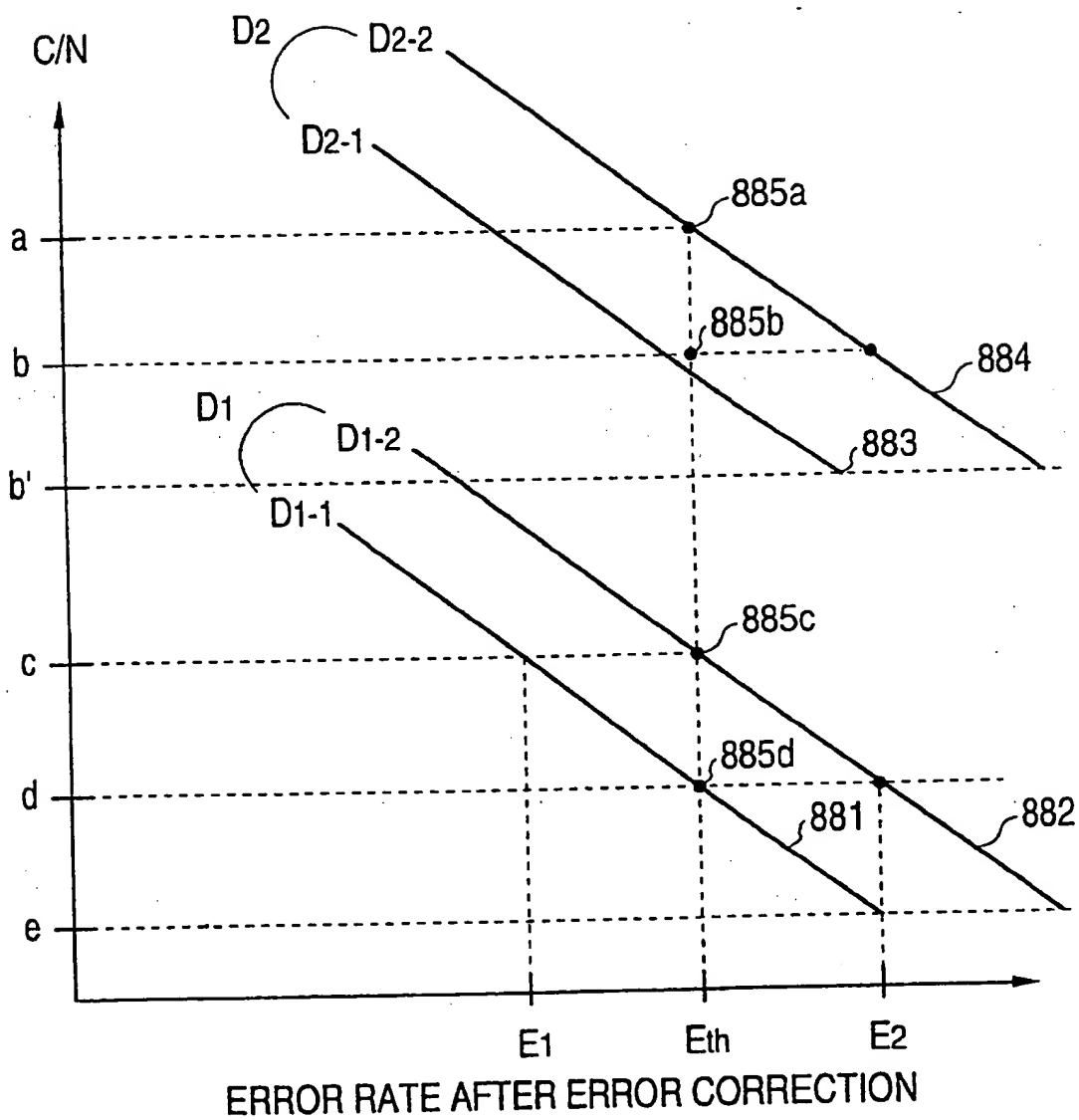


FIG. 90

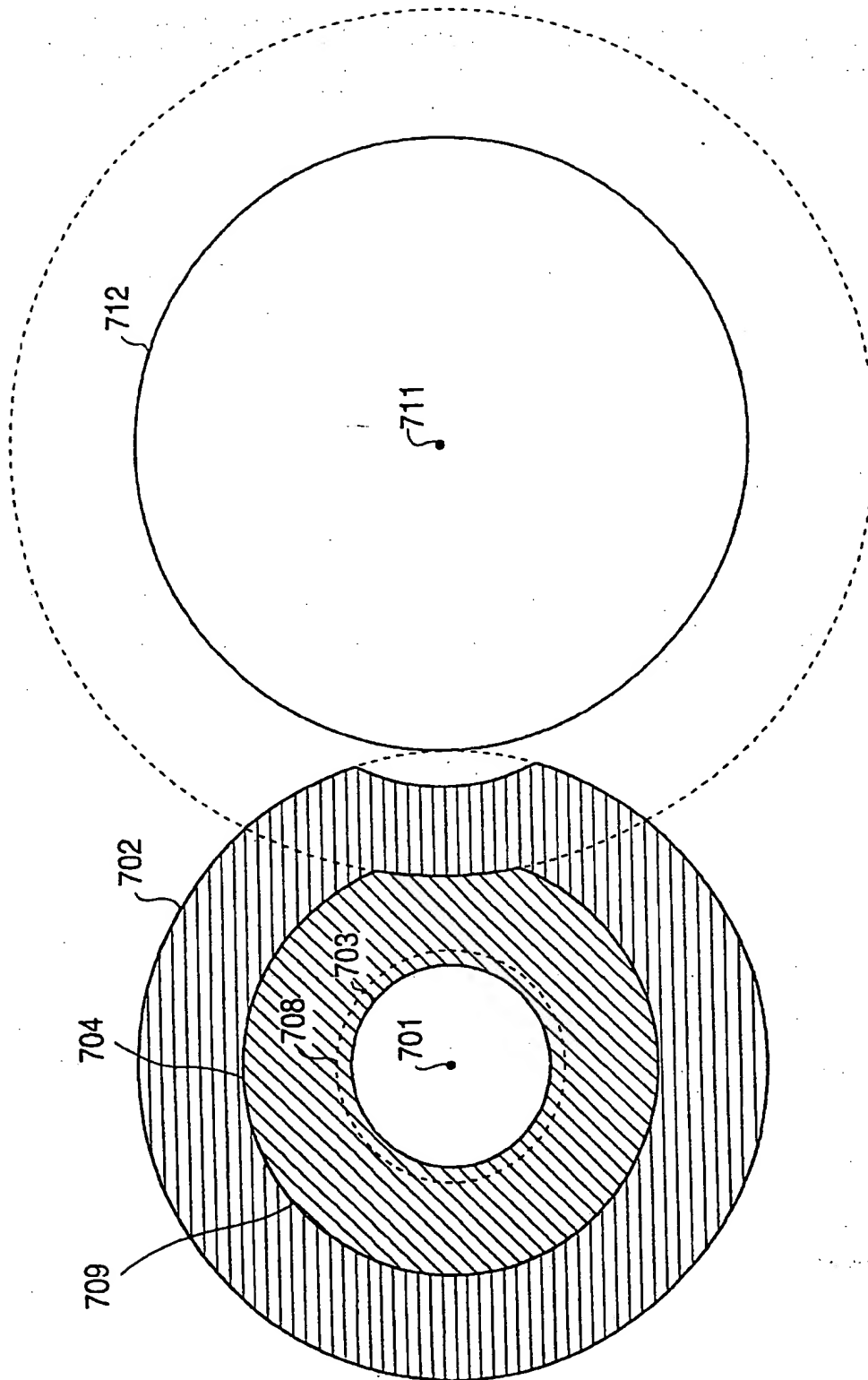


FIG. 91

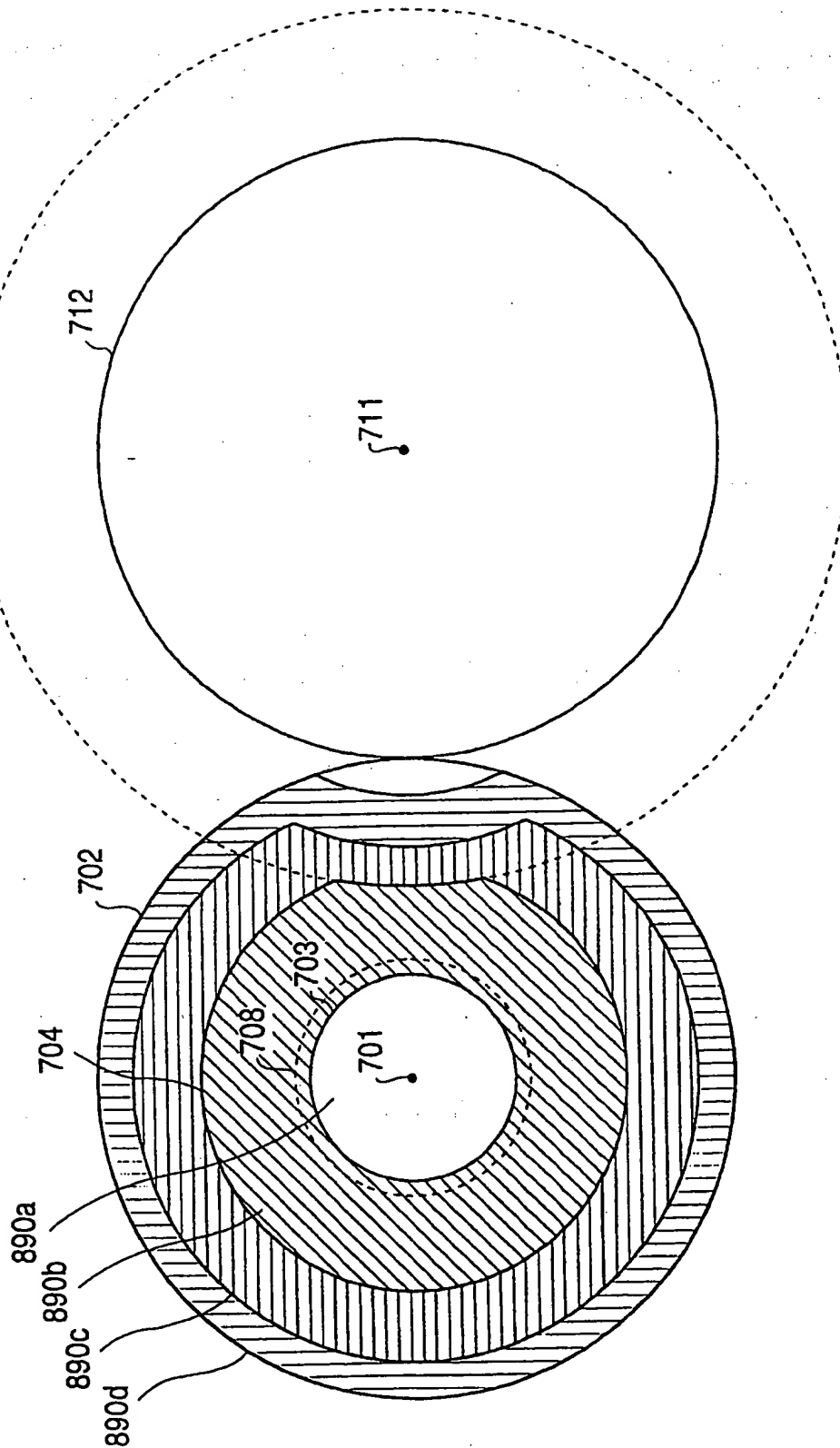


FIG. 92

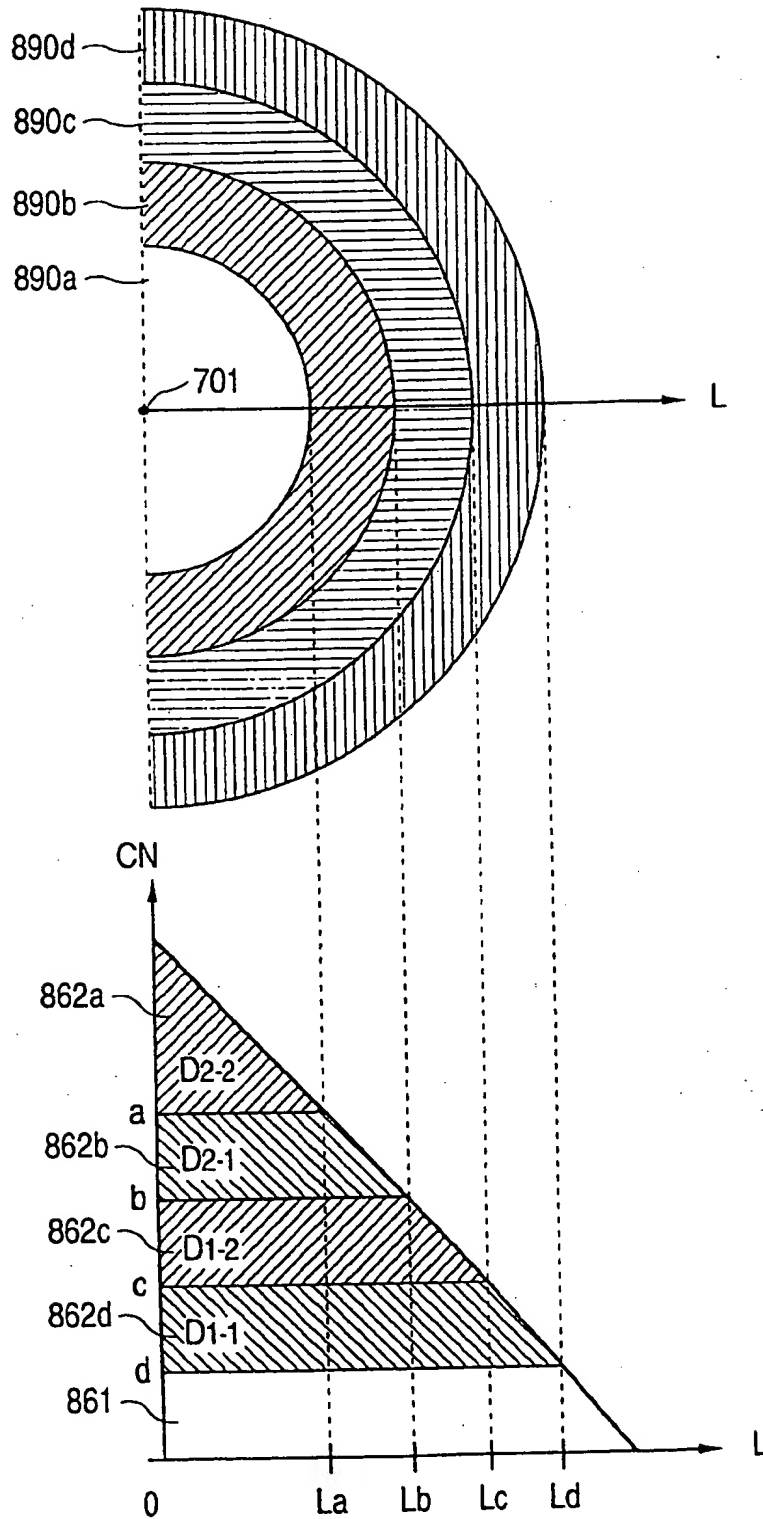


FIG. 93

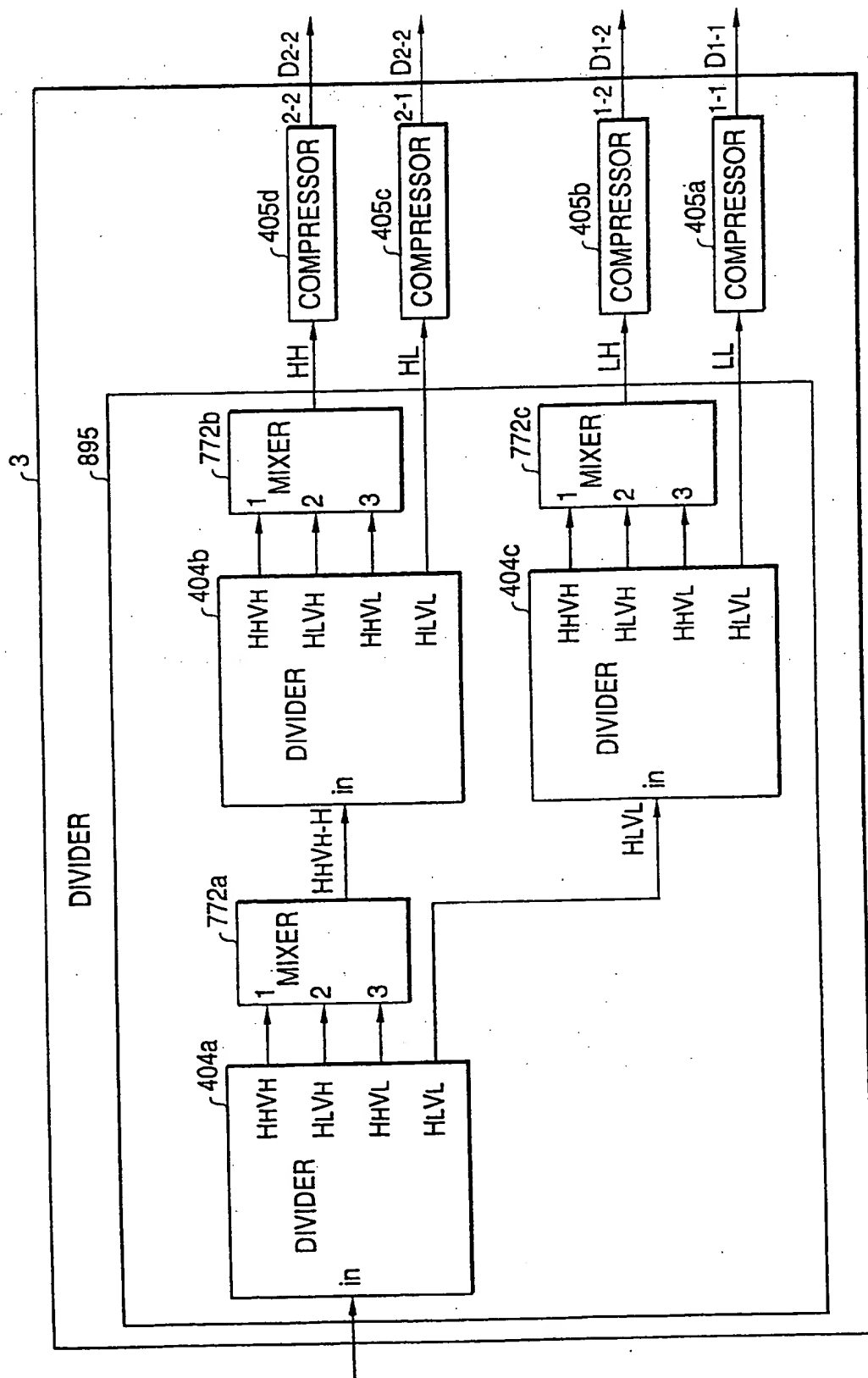


FIG. 94

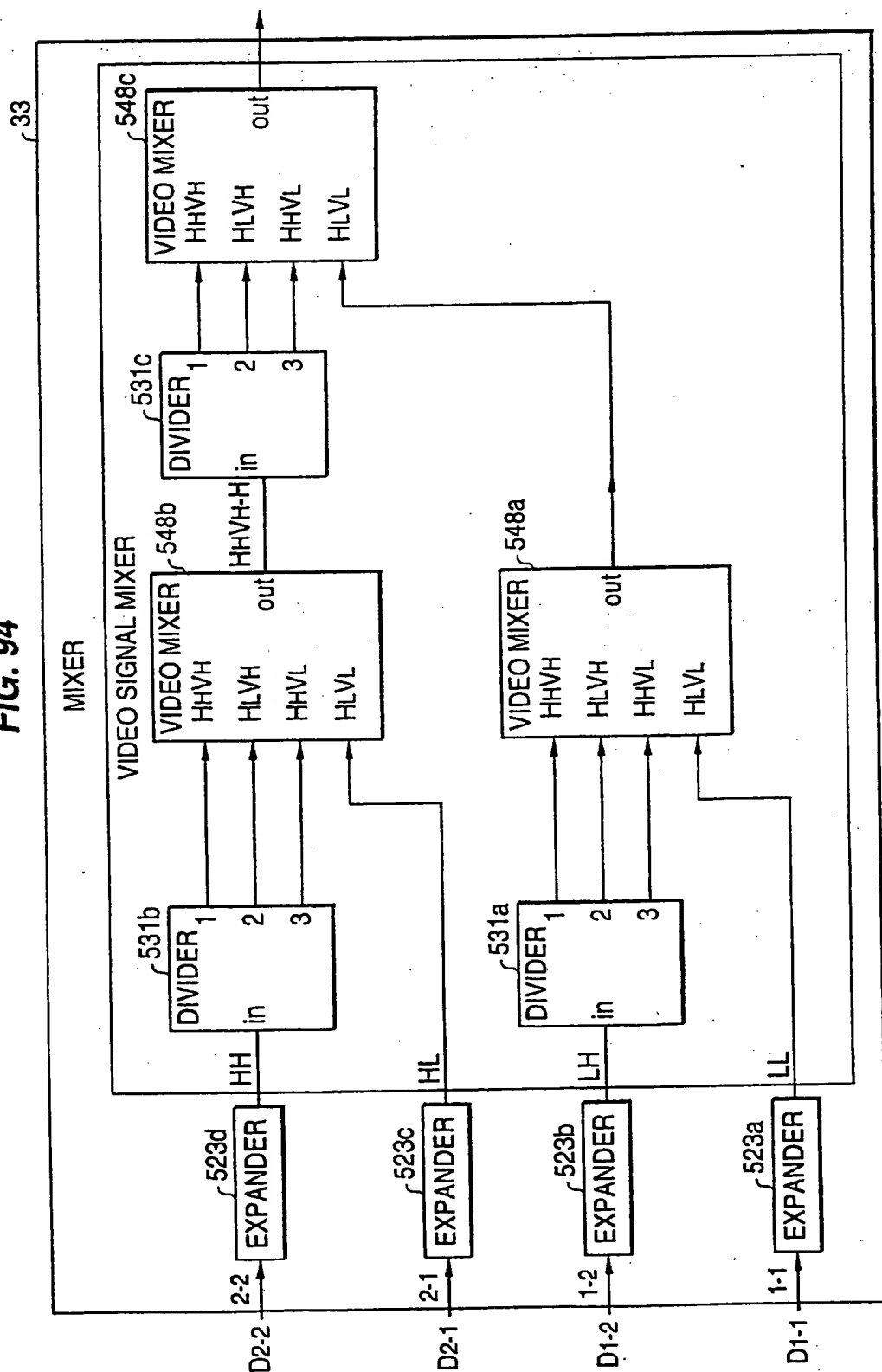


FIG. 95

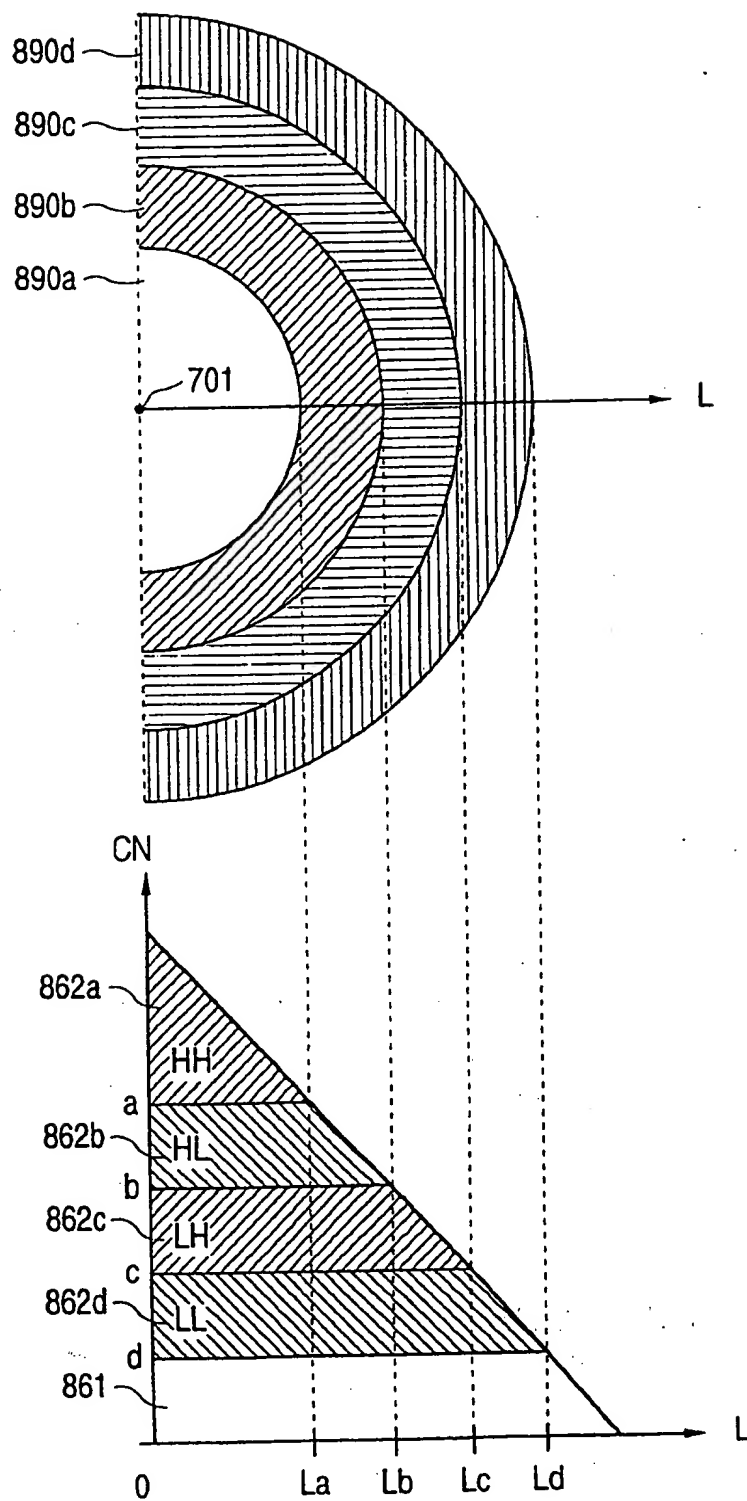


FIG. 96

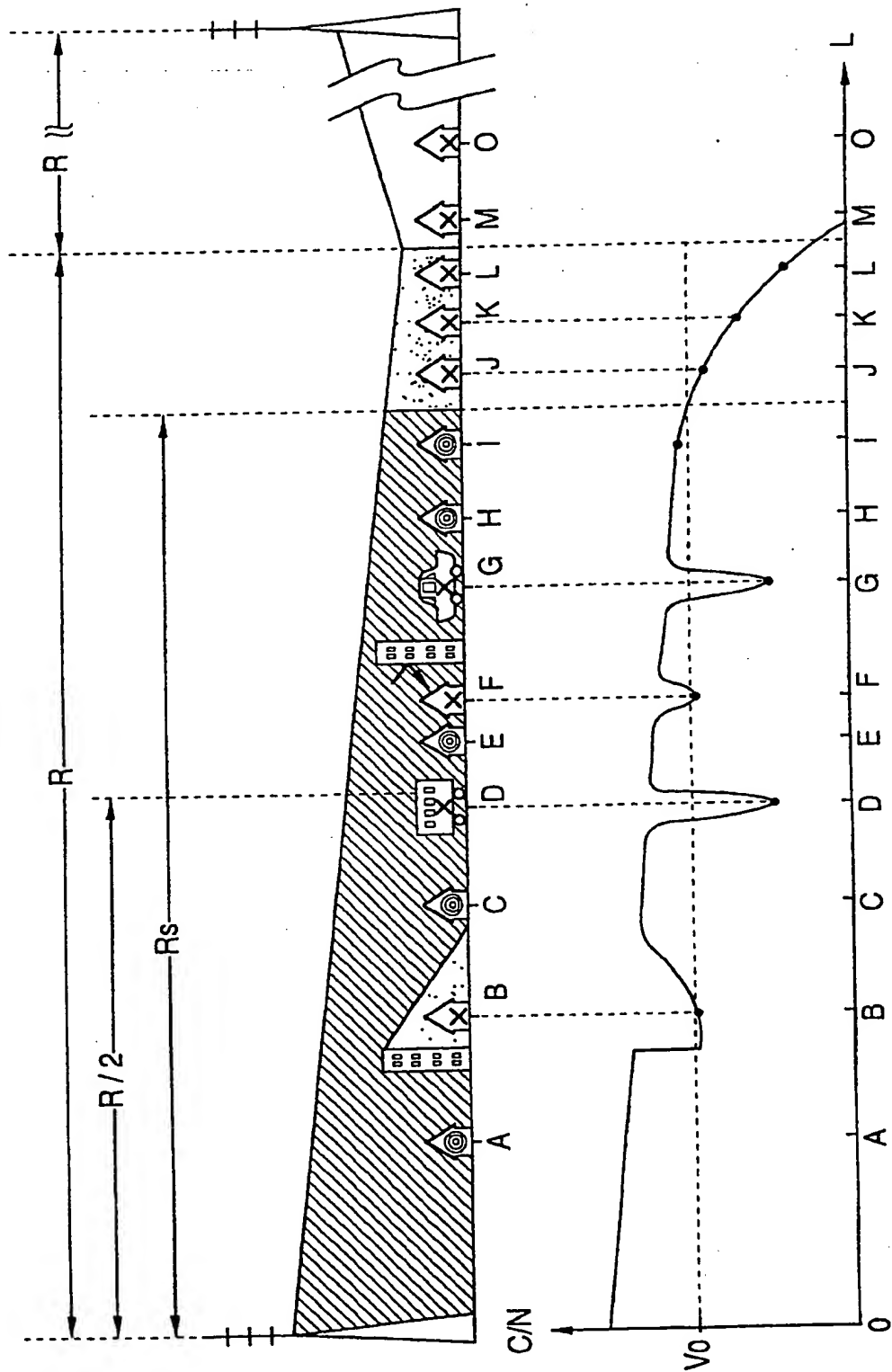


FIG. 98

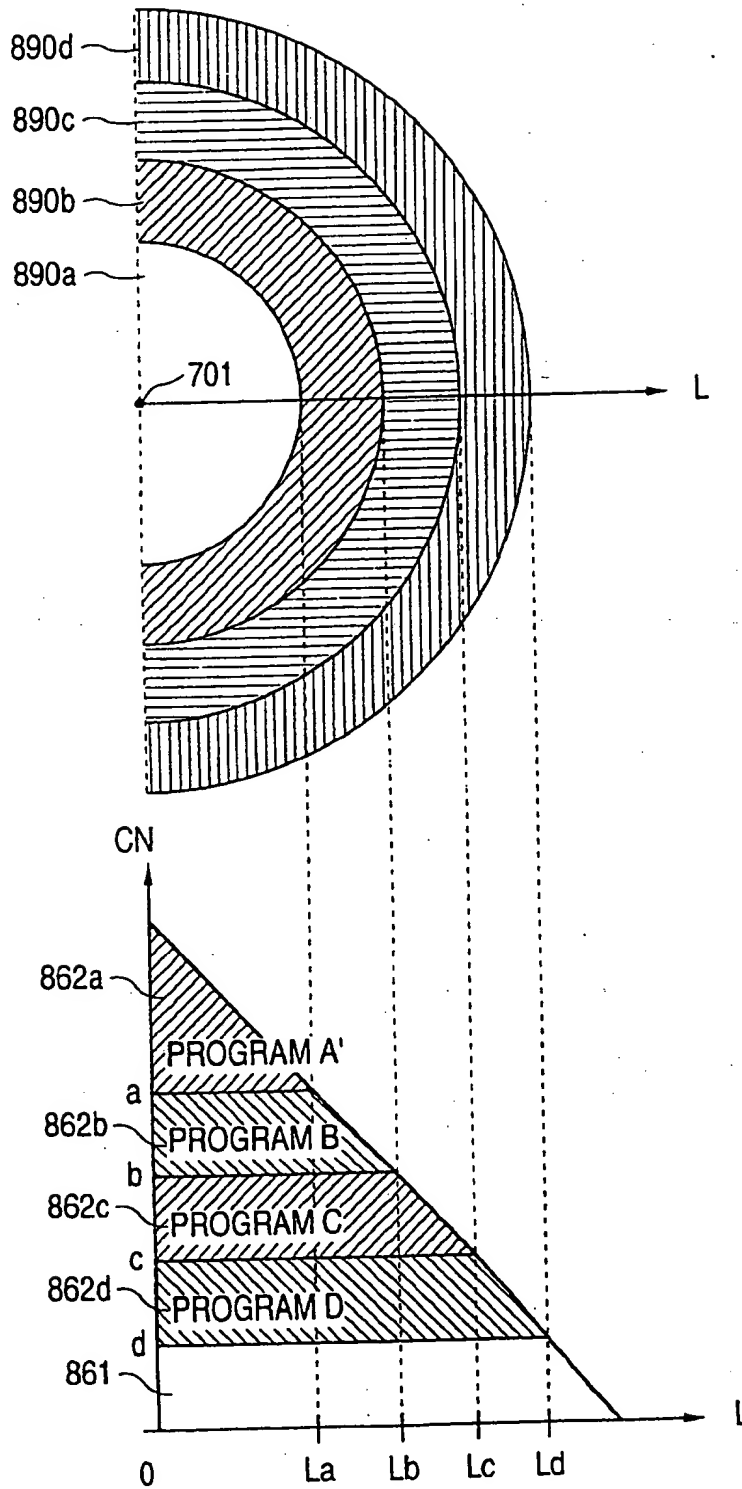


FIG. 99

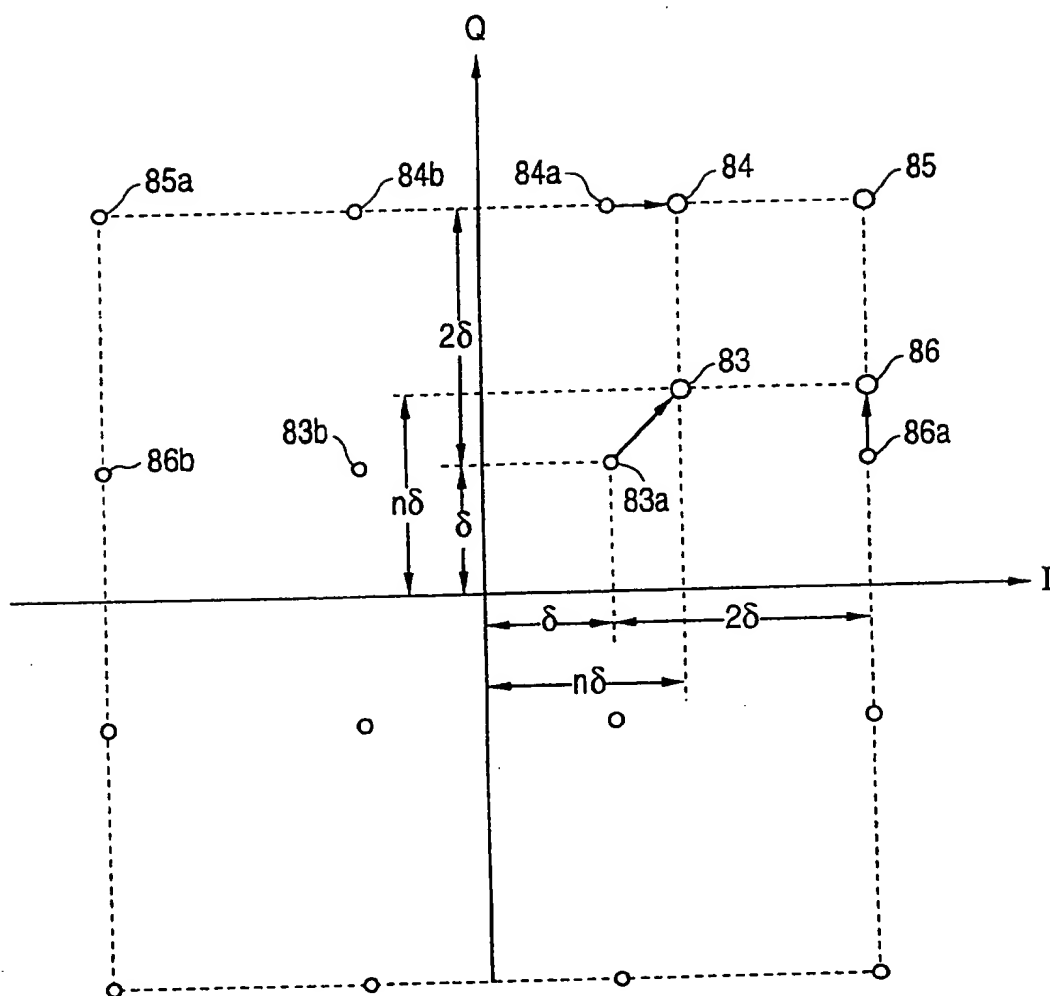


FIG. 100

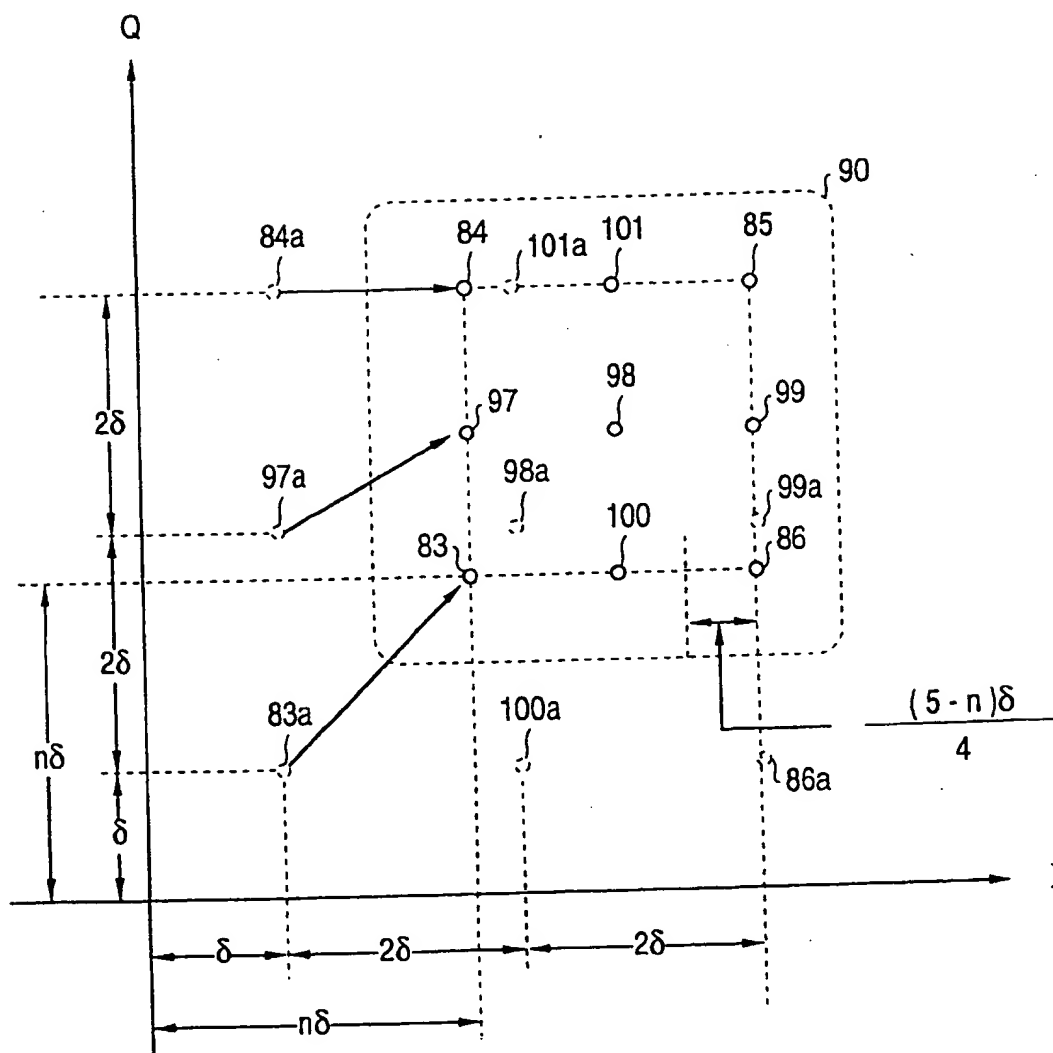
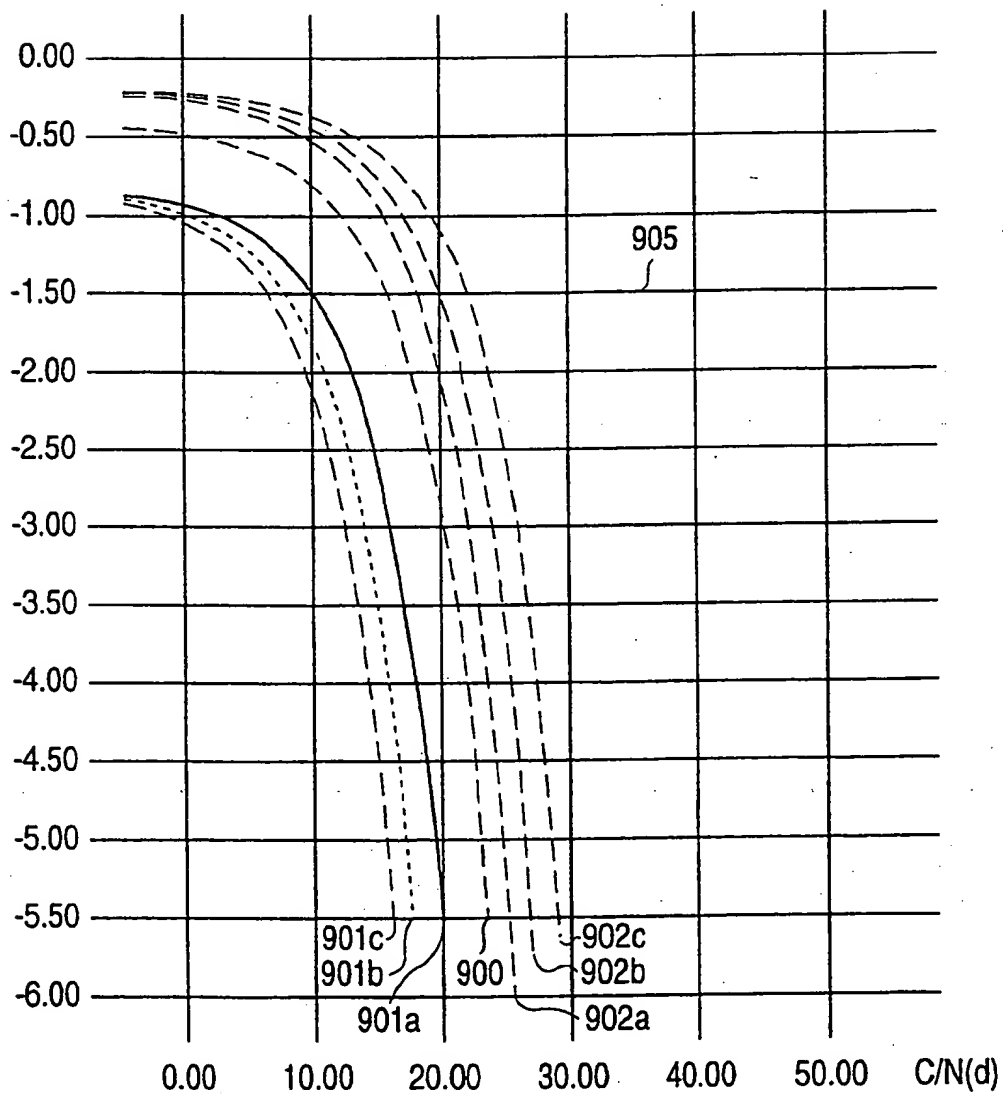


FIG. 101

Pe



Pe

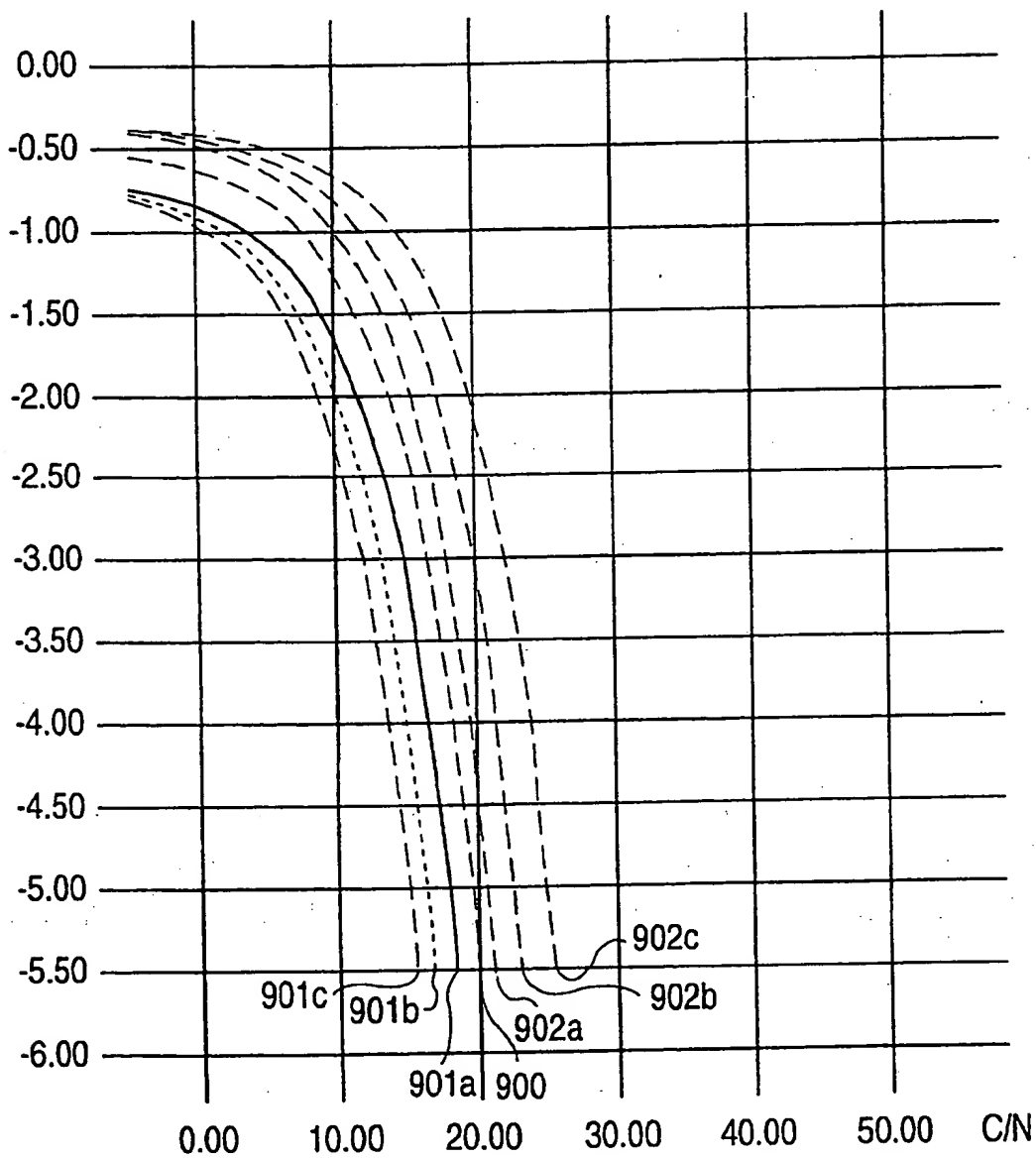


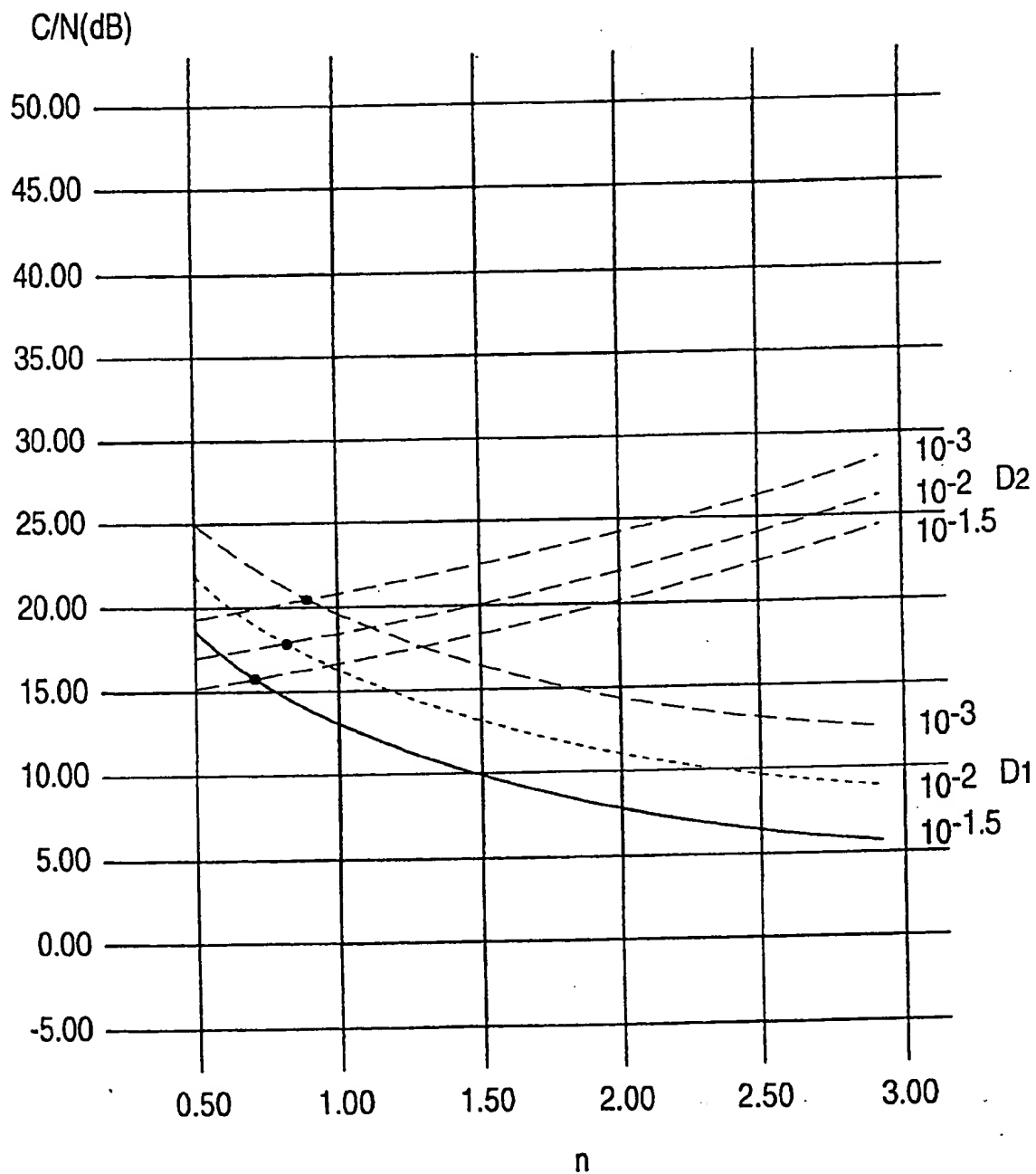
FIG. 103

FIG. 104

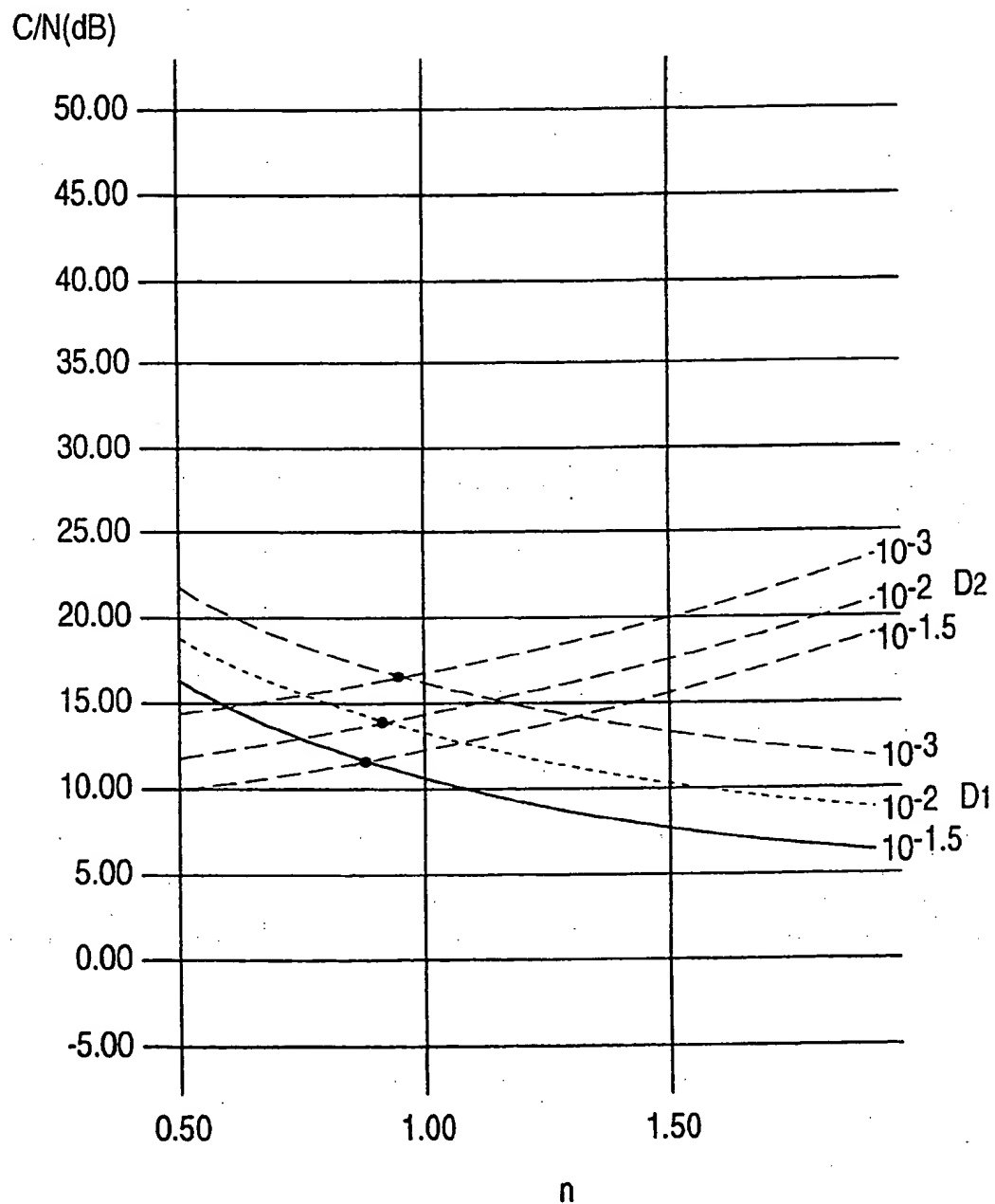


FIG. 105

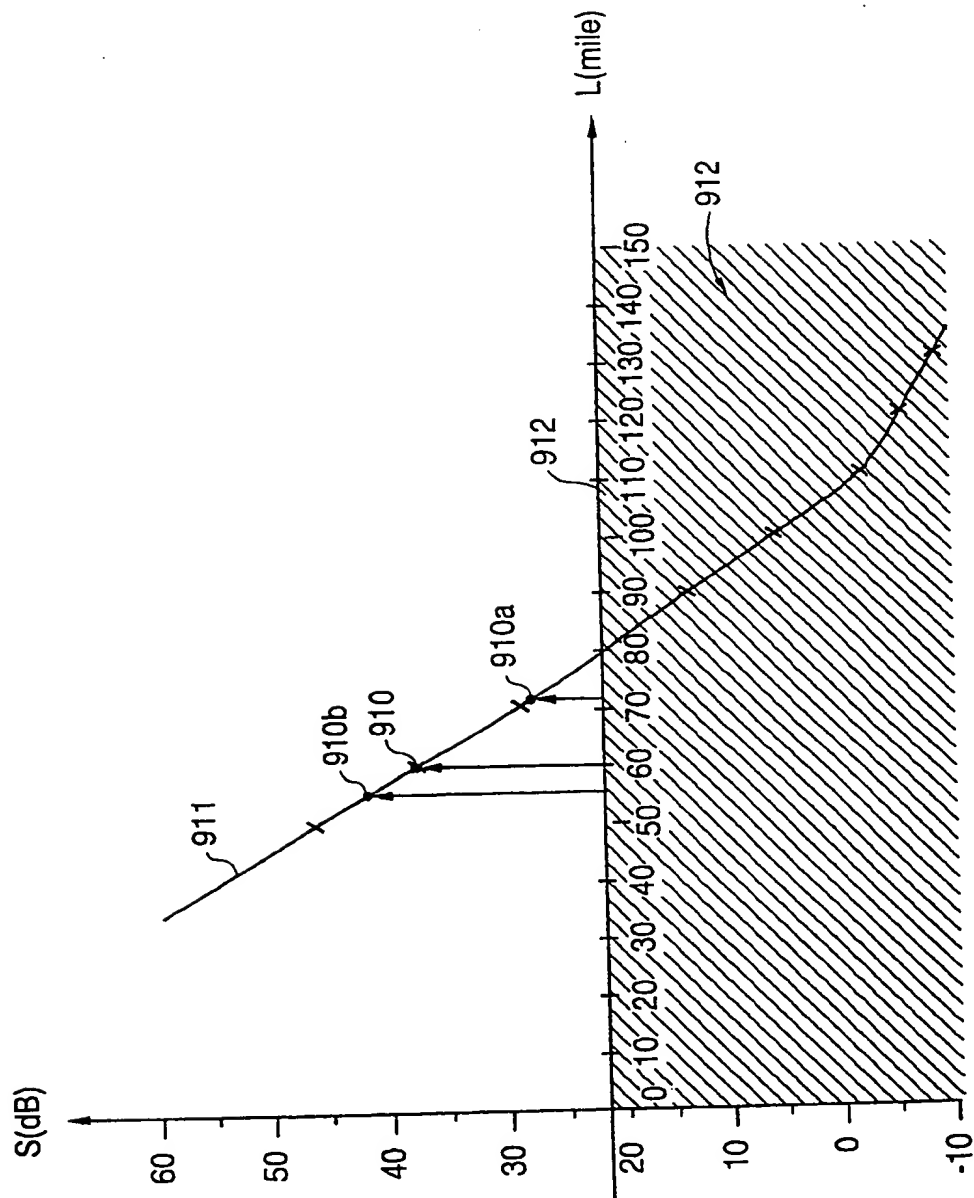


FIG. 107

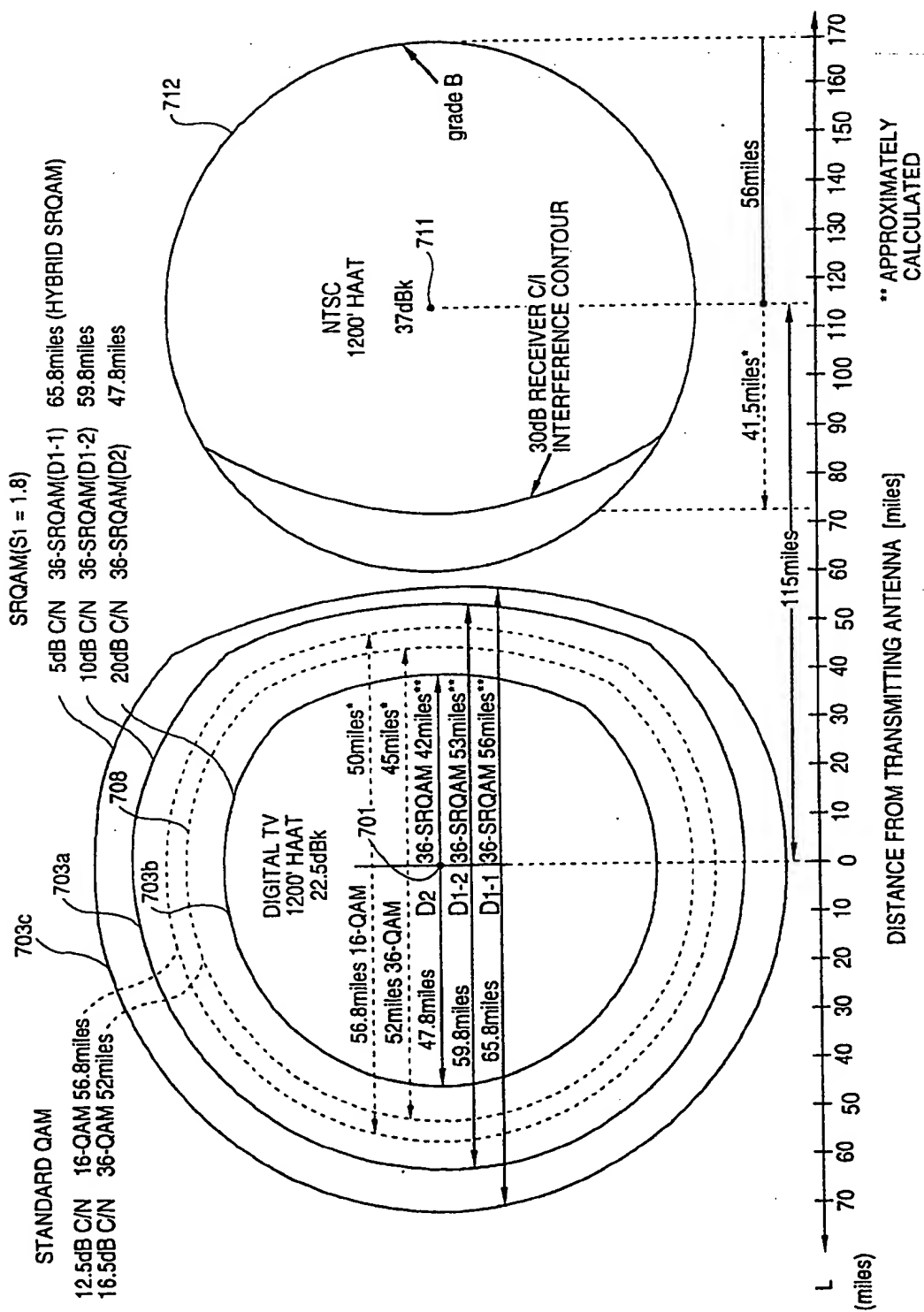


FIG. 108(a)

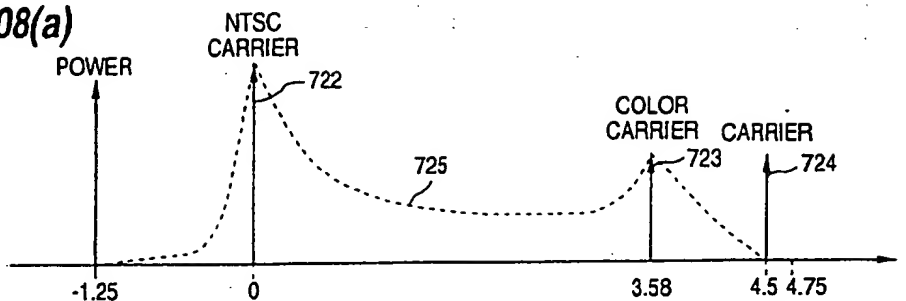


FIG. 108(b)

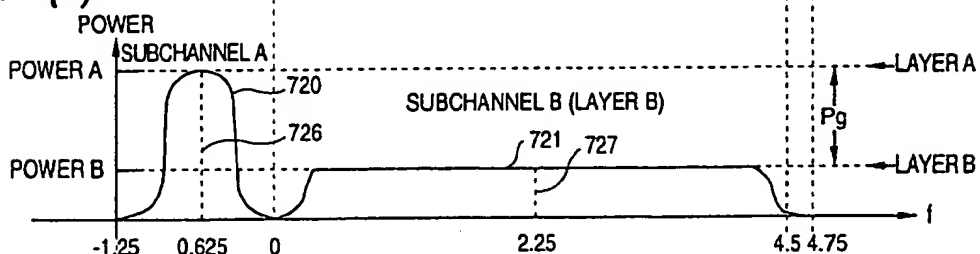


FIG. 108(c)

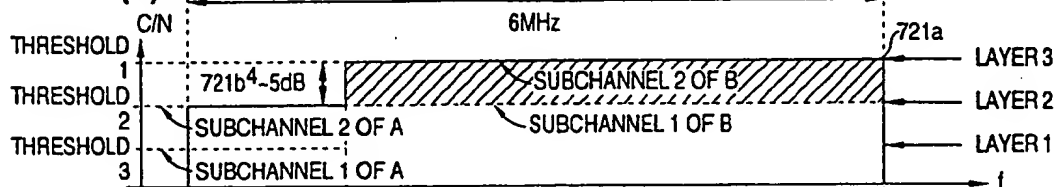


FIG. 108(d)

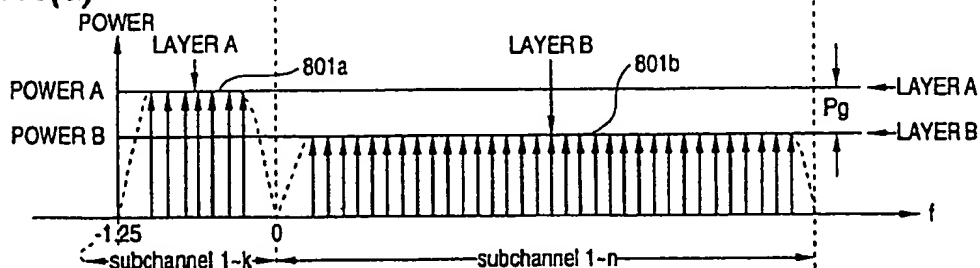


FIG. 108(e)

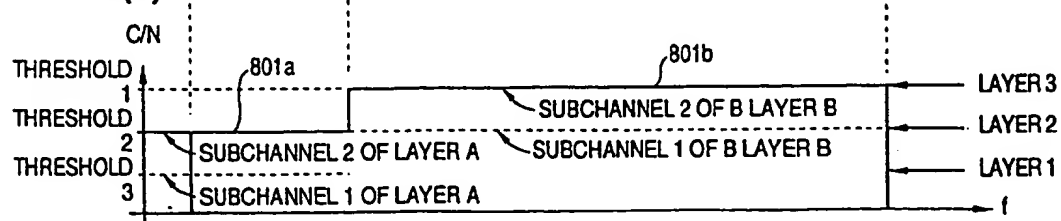


FIG. 109

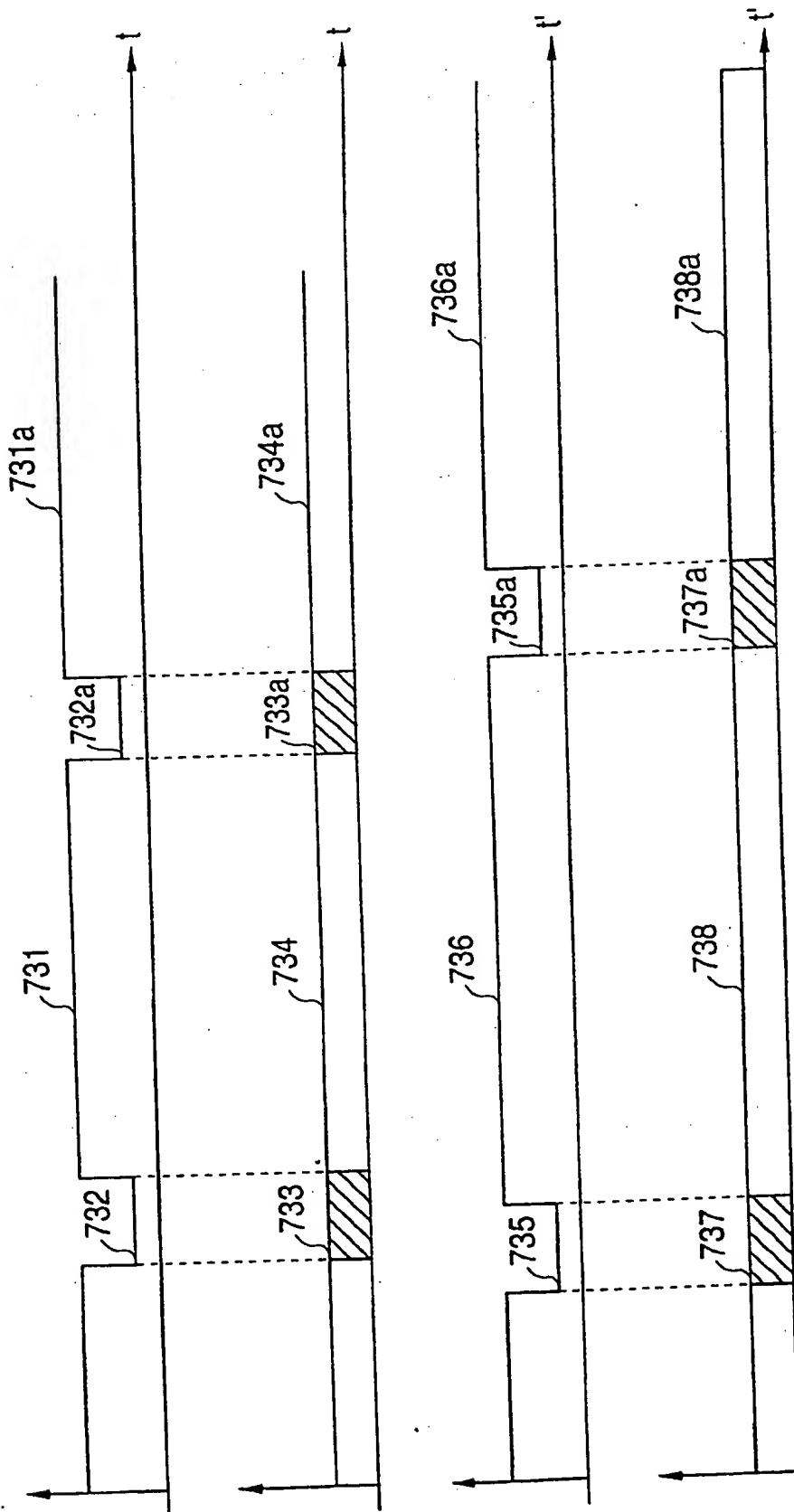
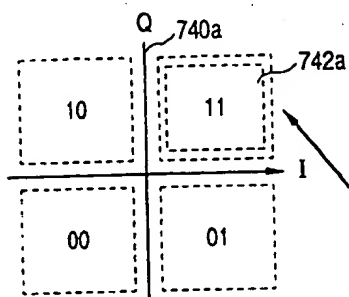


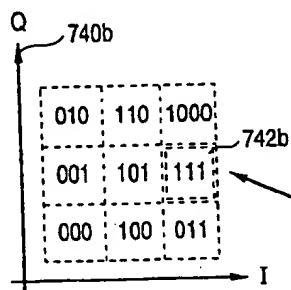
FIG. 111

SUBCHANNEL-1 (SRQAM:D1 = 2bit)



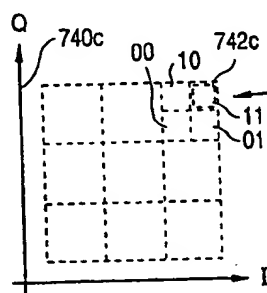
CODE WORD-1

SUBCHANNEL-2 (36-SRQAM:D2 = 3bit + 1/8bit)



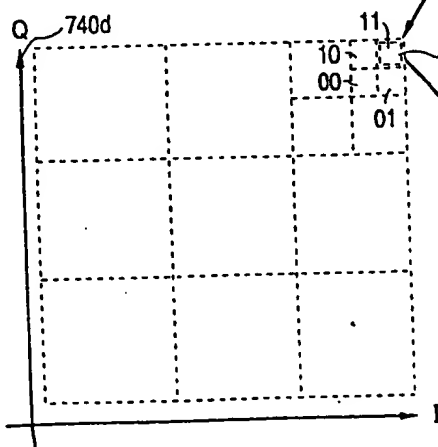
CODE WORD-2

SUBCHANNEL-3 (144-SRQAM:D3 = 2bit)

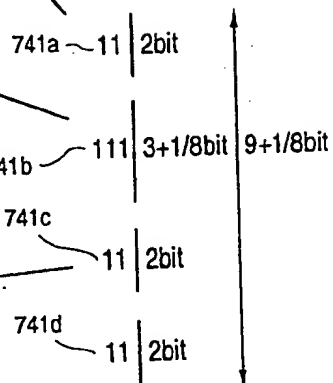


CODE WORD-3

SUBCHANNEL-4 (576-SRQAM:D4 = 2bit)



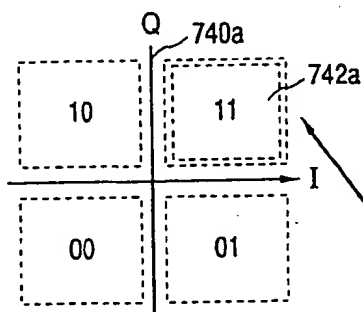
CODE WORD-4



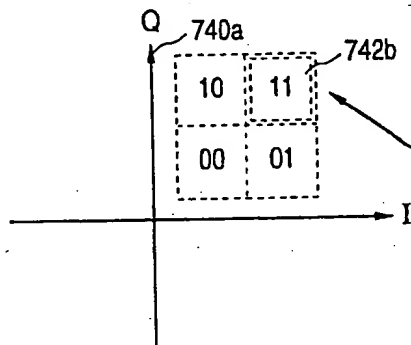
SIGNAL POINT
CODE WORD
11 11 11 11

FIG. 112

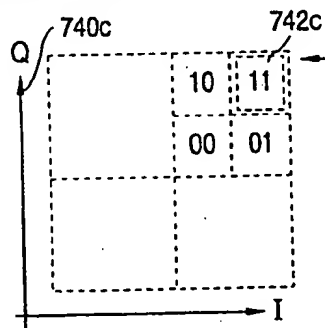
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



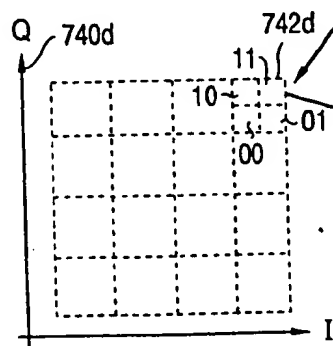
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)



SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)

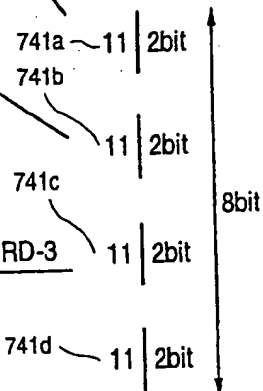


CODE WORD-1

CODE WORD-2

CODE WORD-3

CODE WORD-4



SIGNAL POINT
CODE WORD
11 11 11 11

FIG. 113

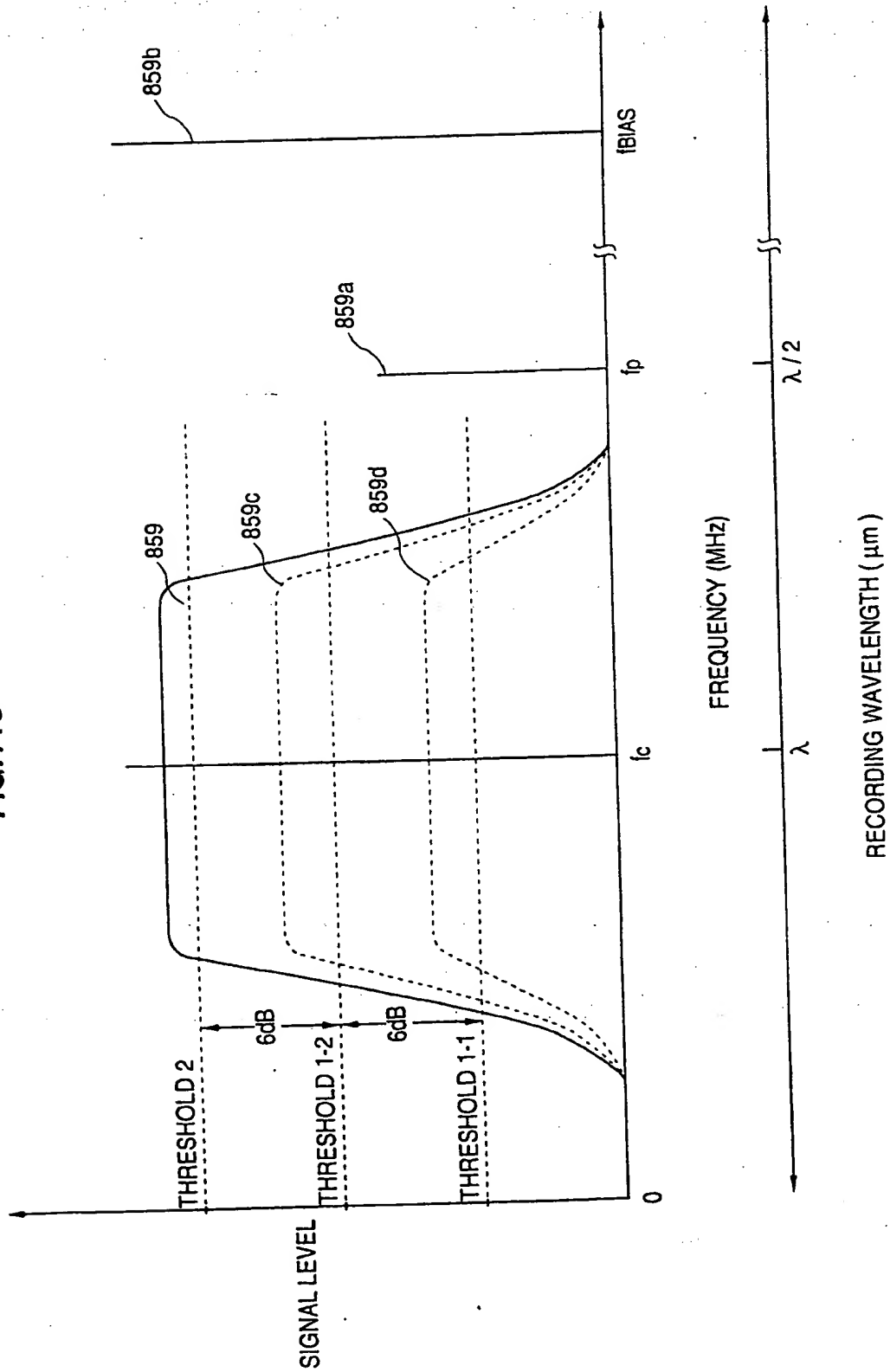


FIG. 114

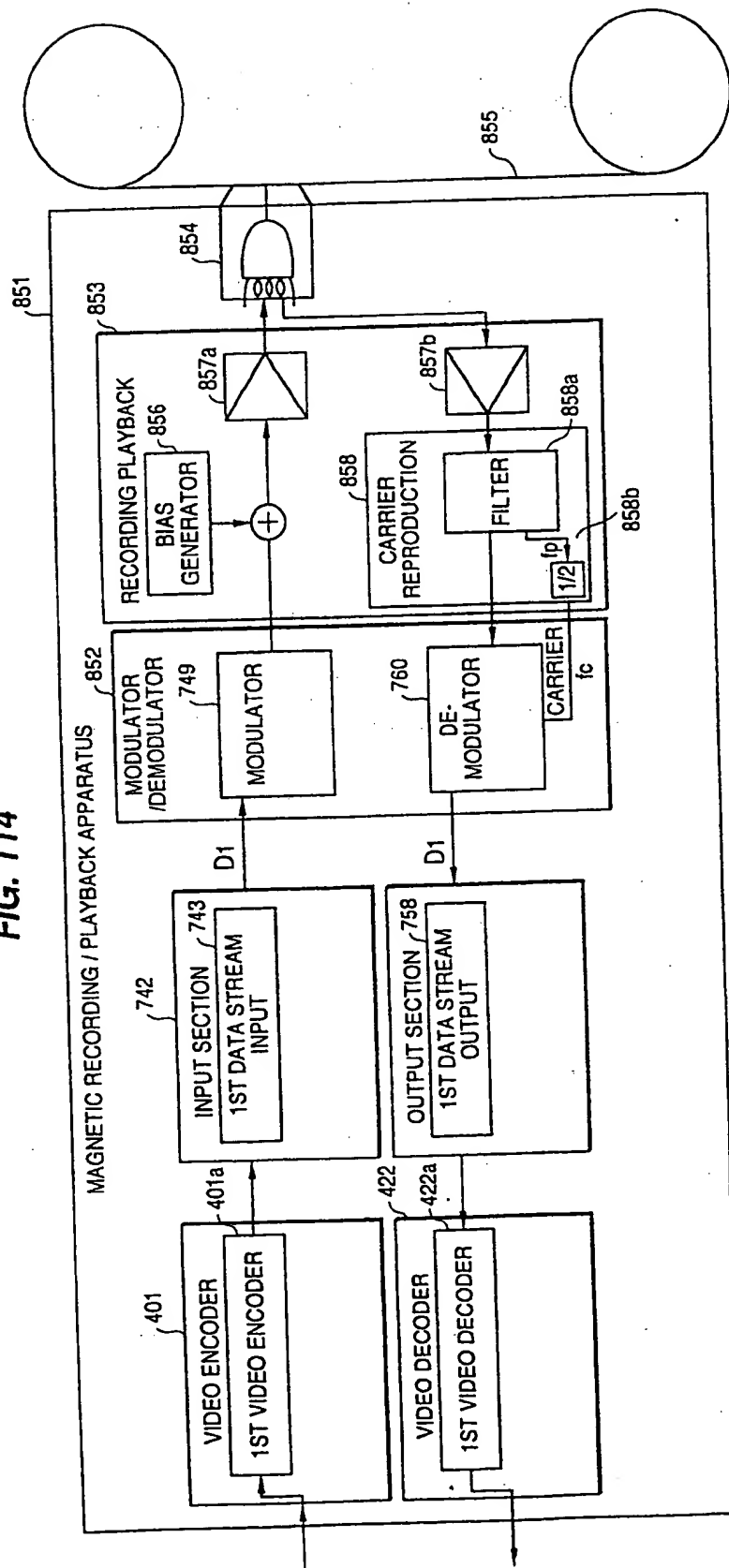


FIG. 115

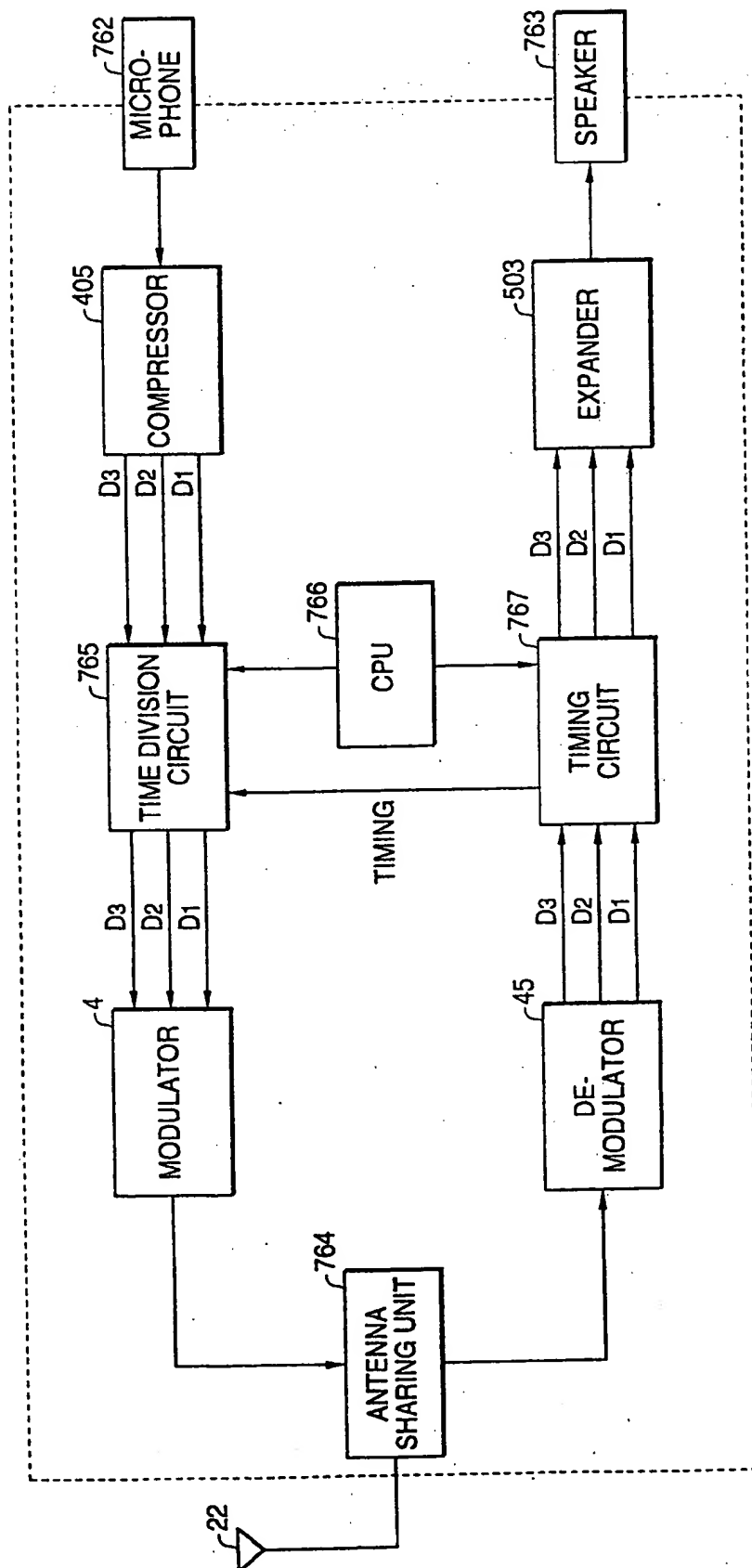


FIG. 116

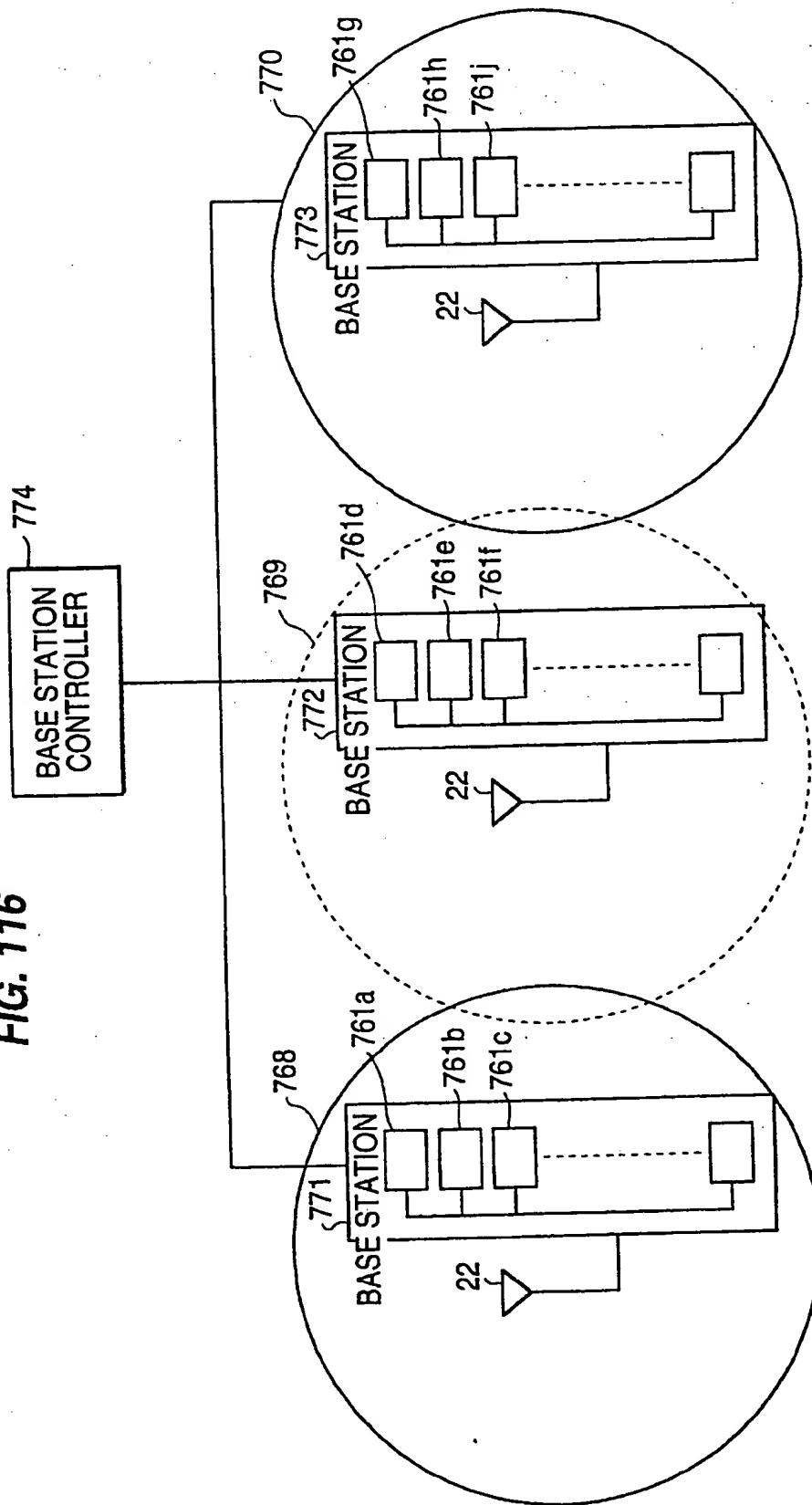


FIG. 117

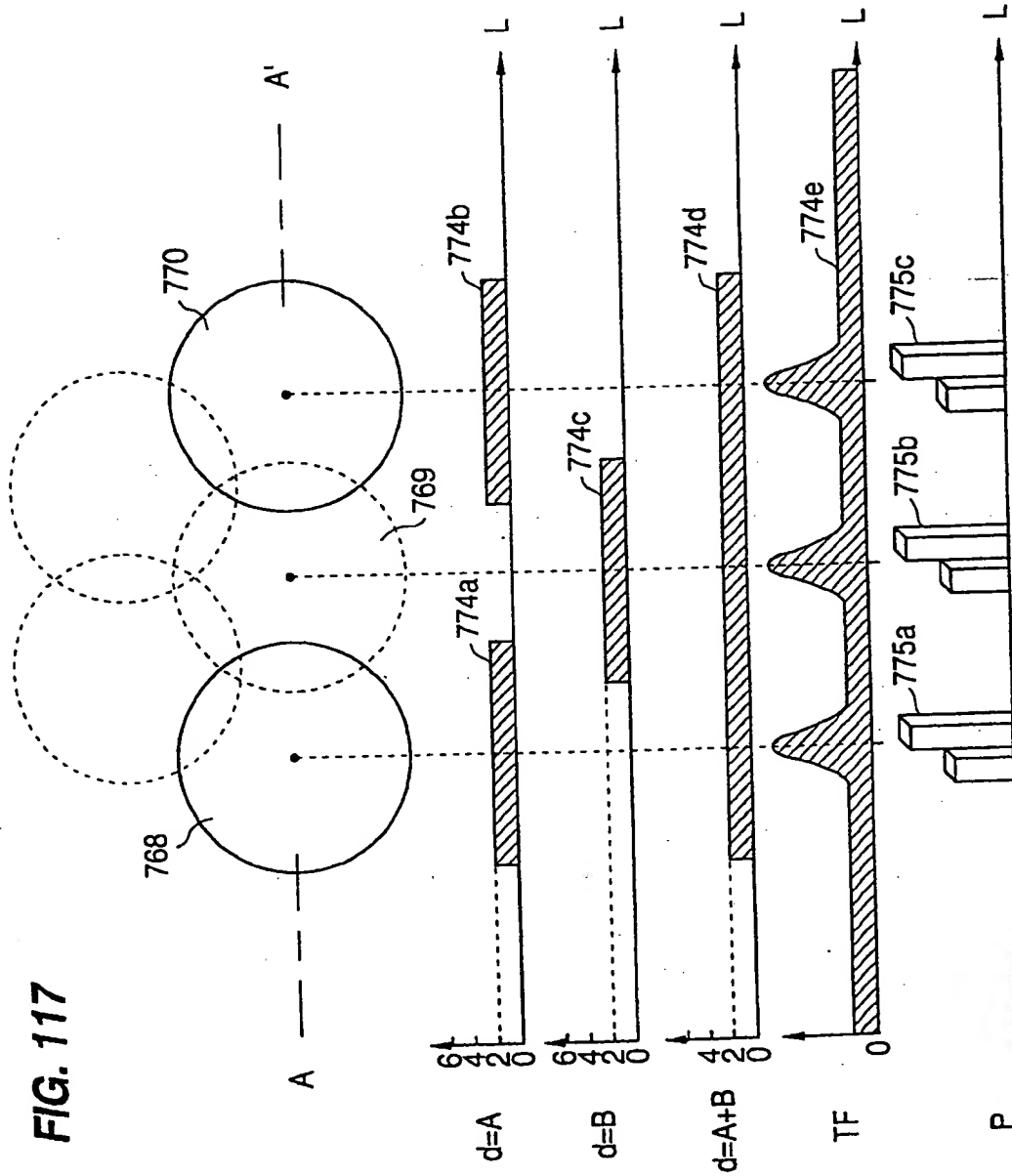
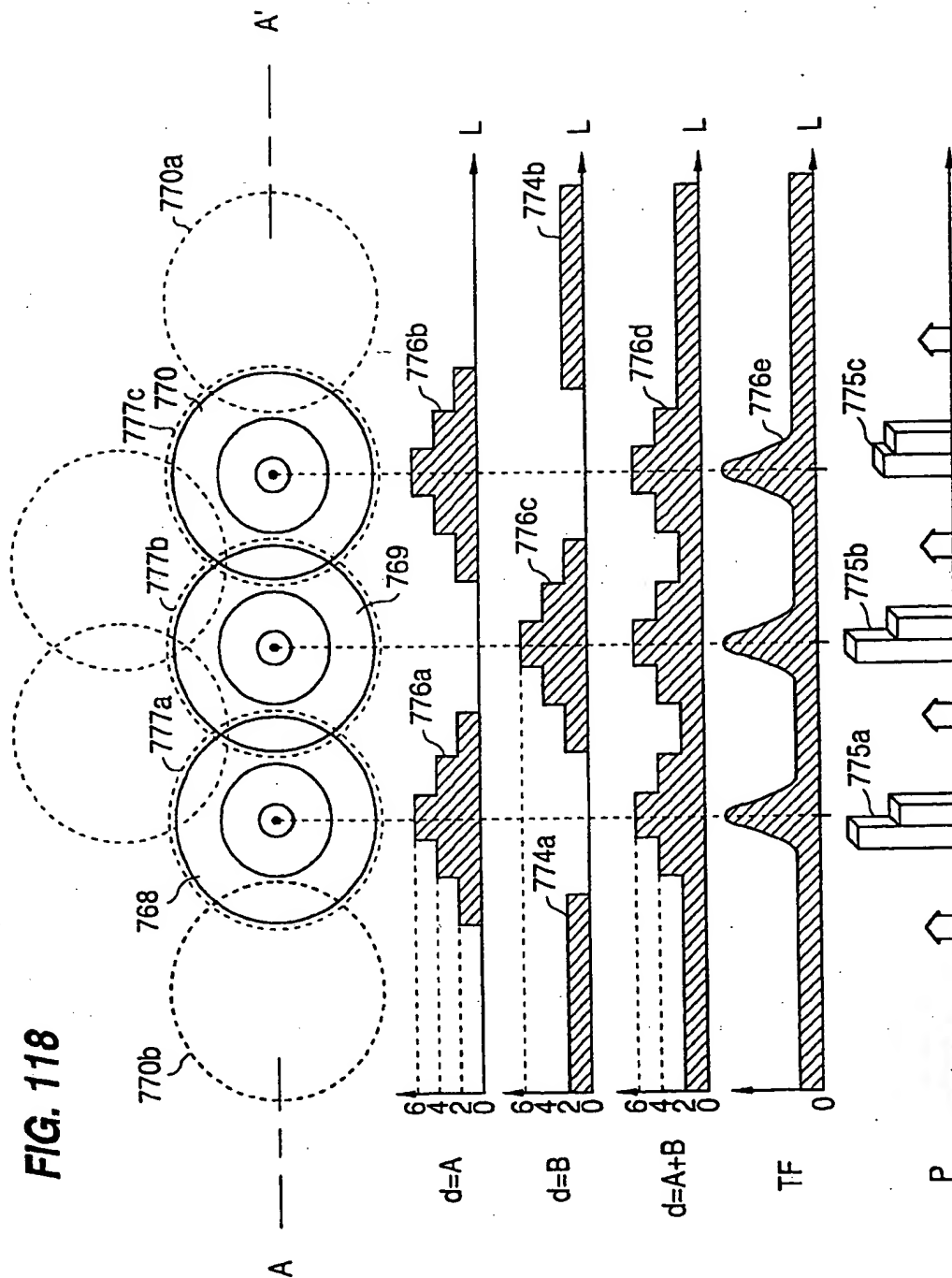


FIG. 118



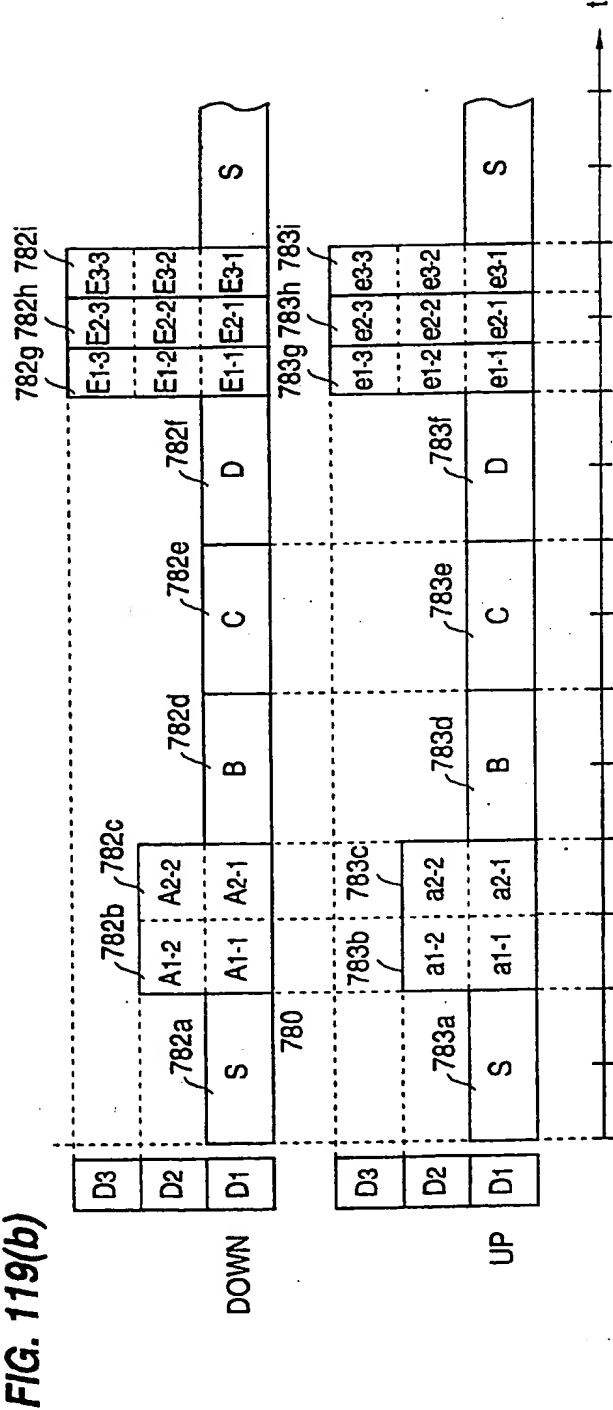
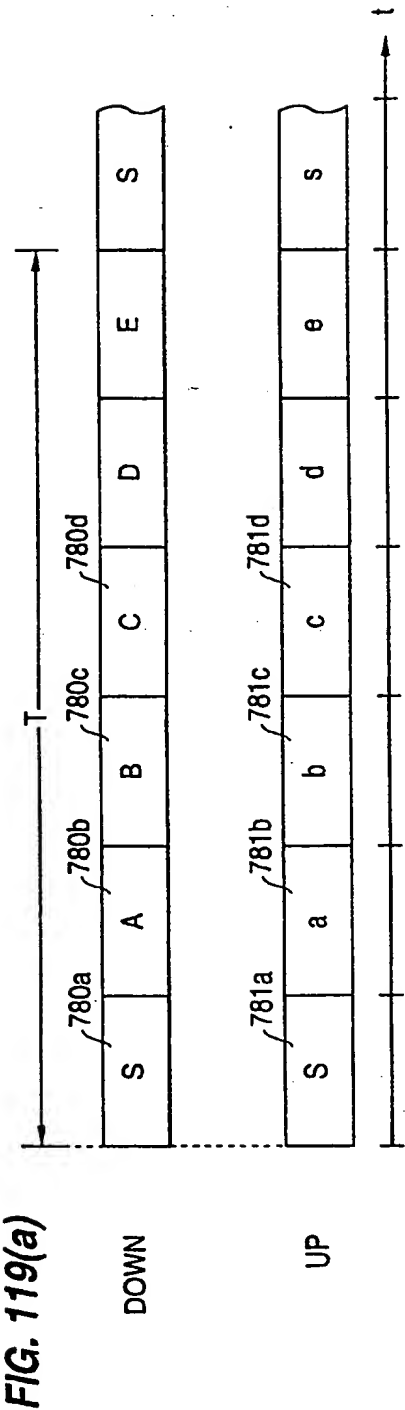


FIG. 120(a)

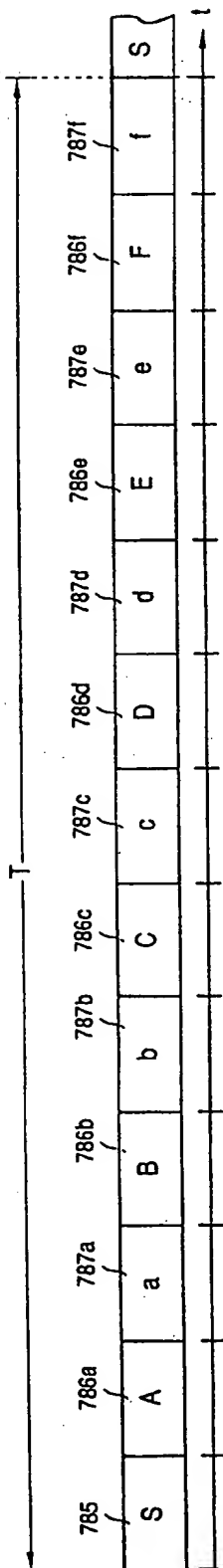


FIG. 120(b)

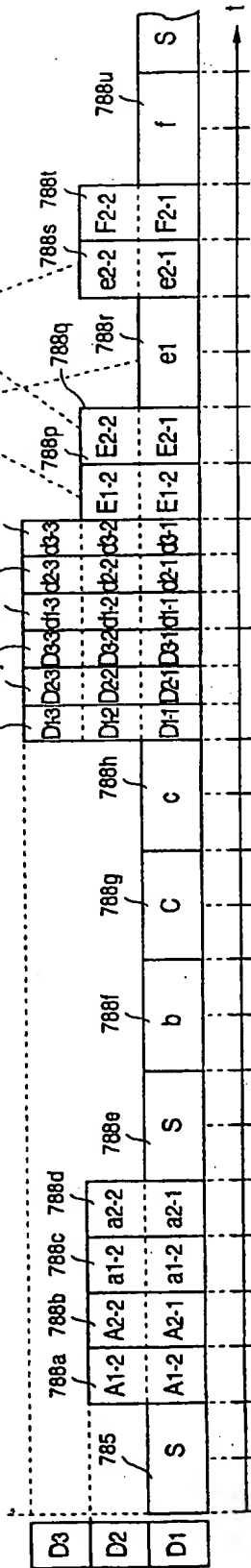


FIG. 121

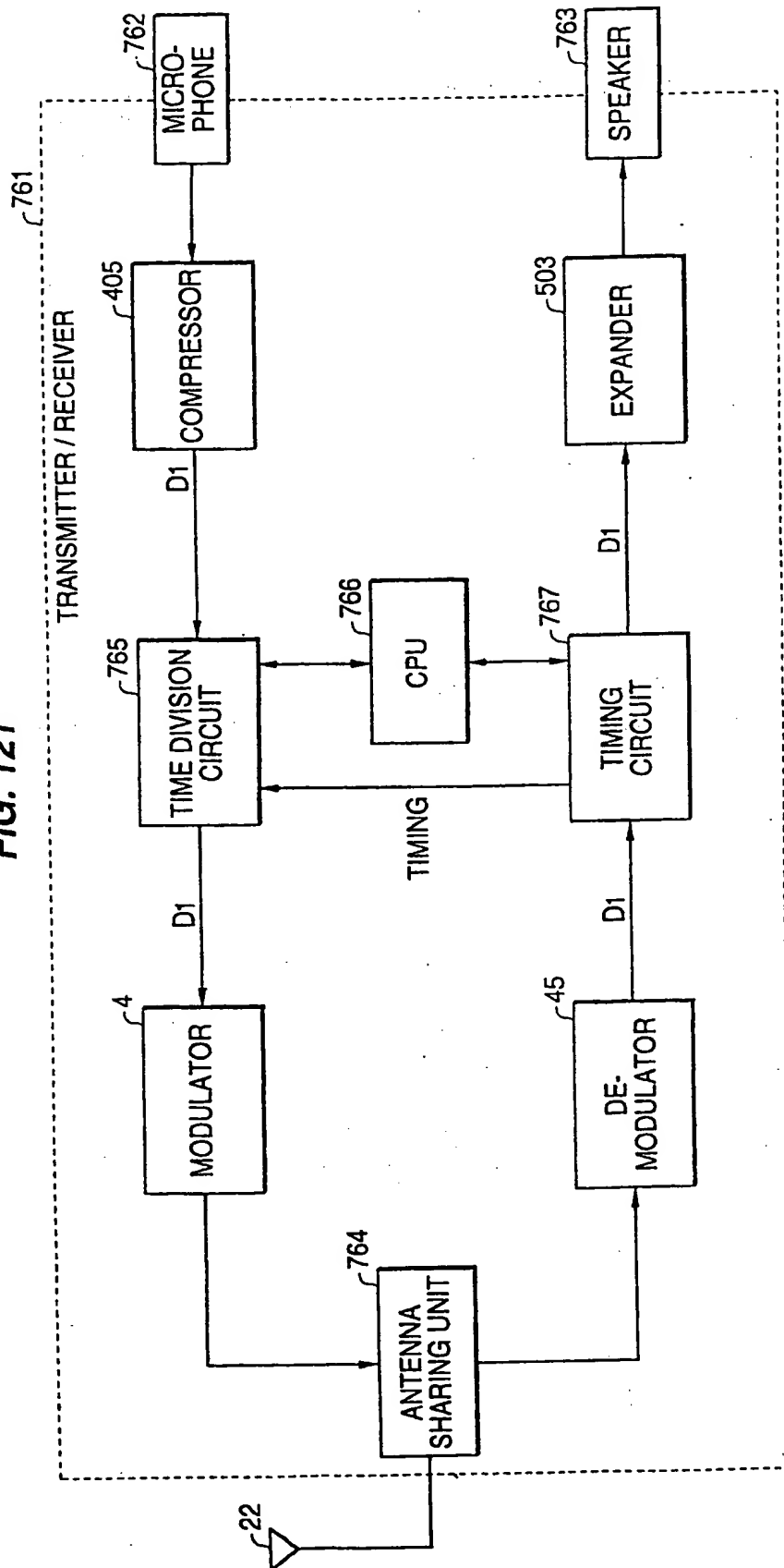


FIG. 122

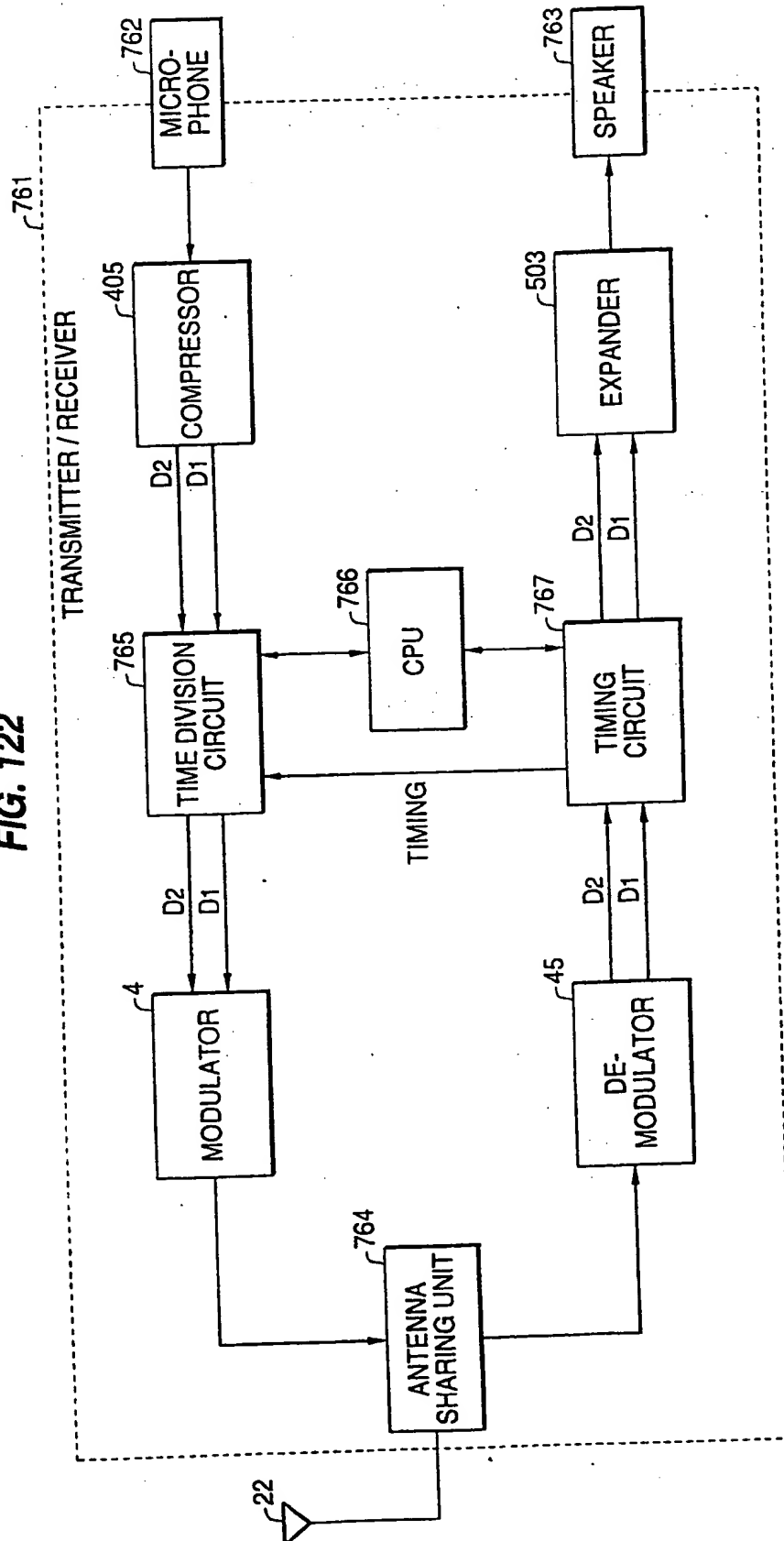
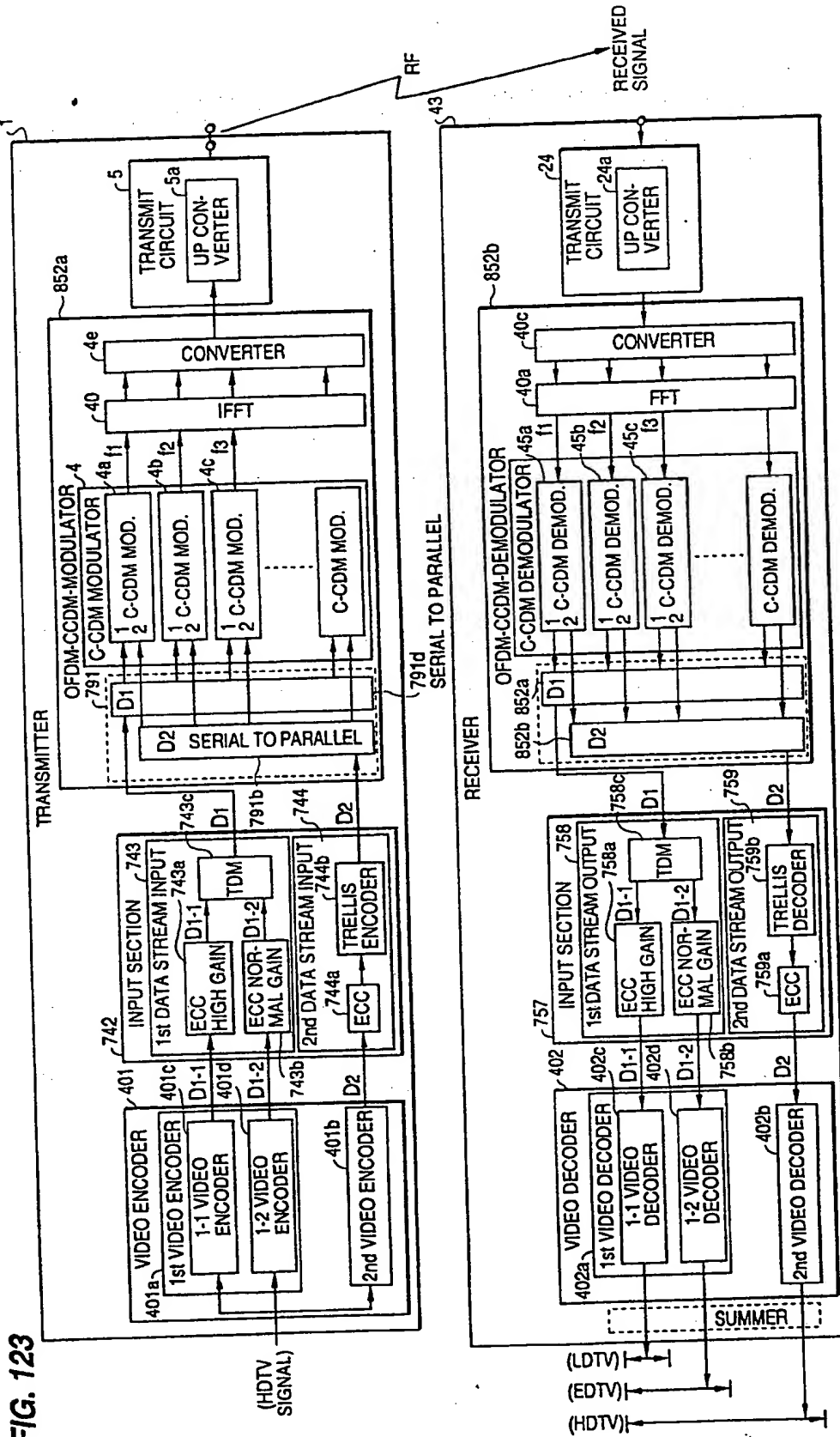


FIG. 123



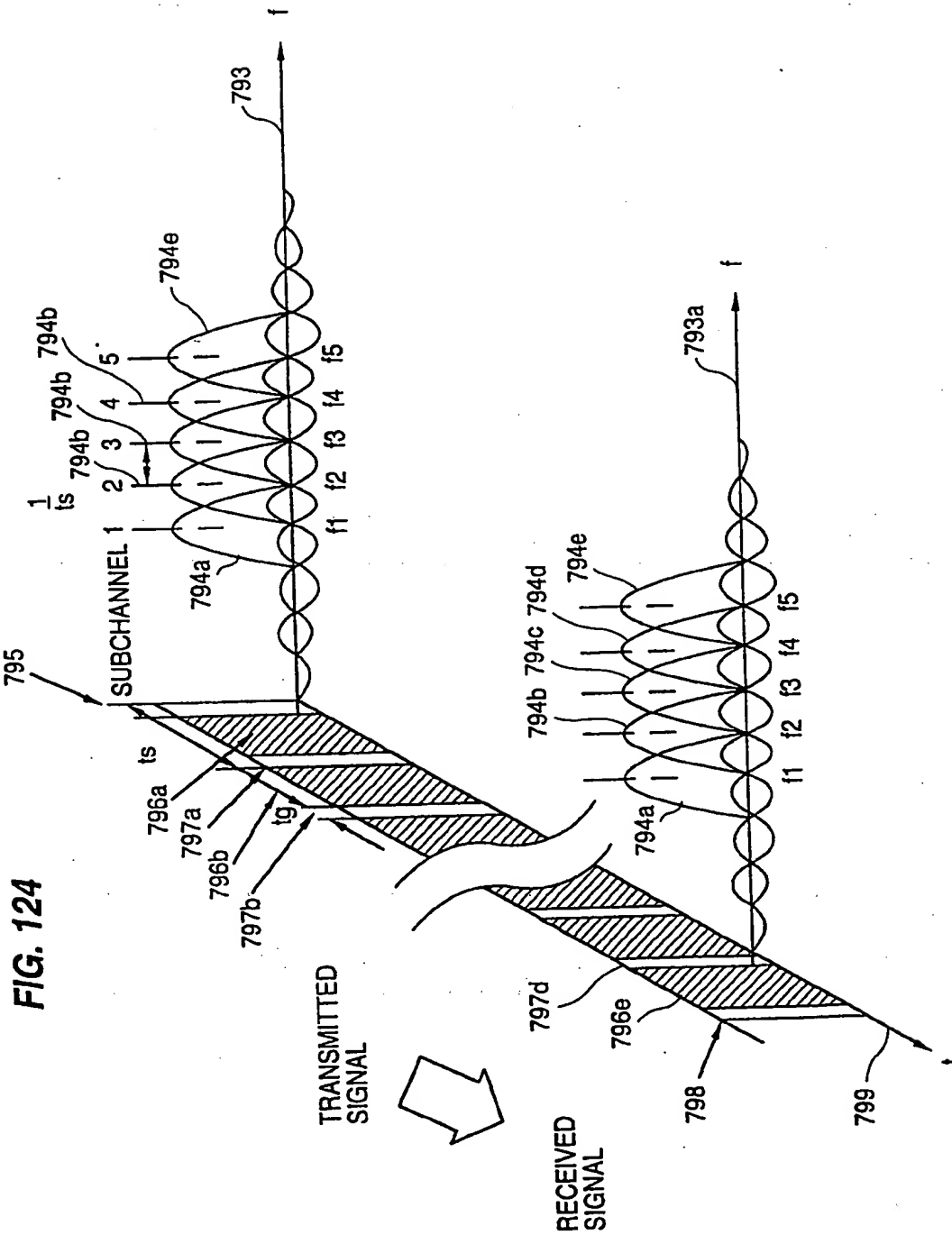


FIG. 125(a)

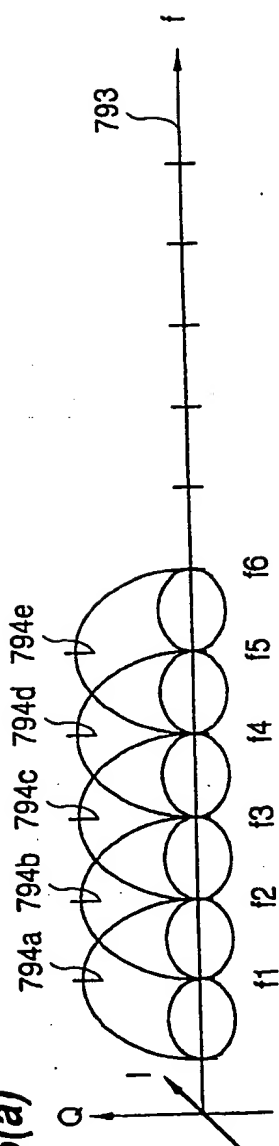
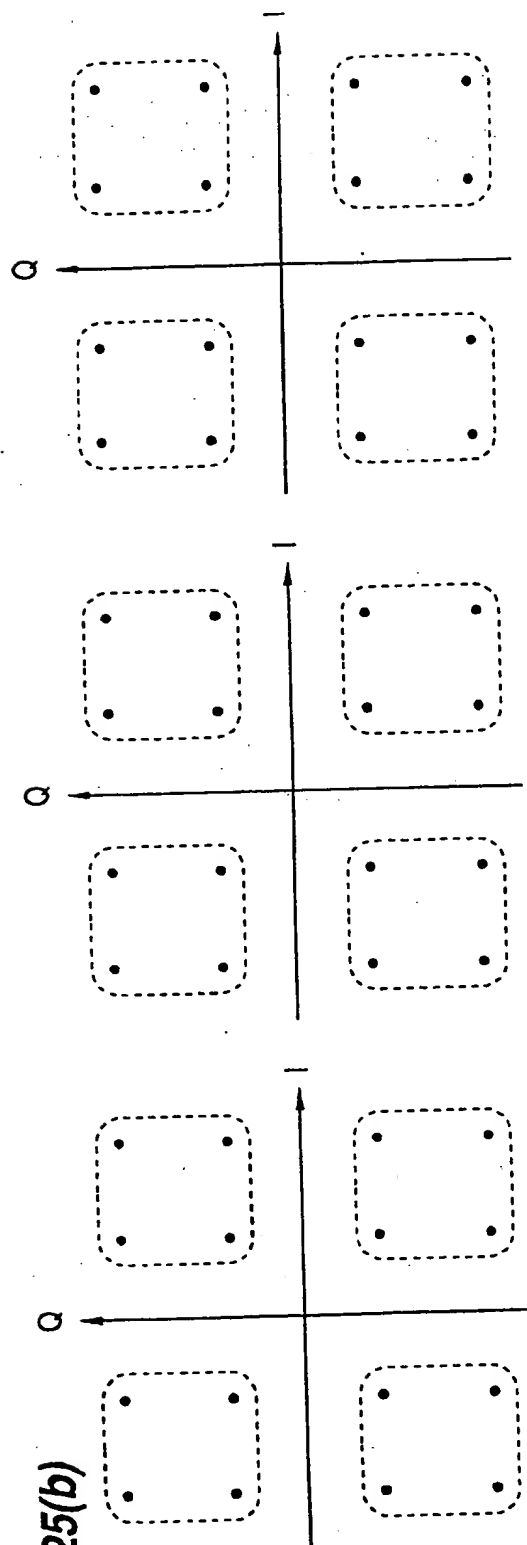


FIG. 125(b)



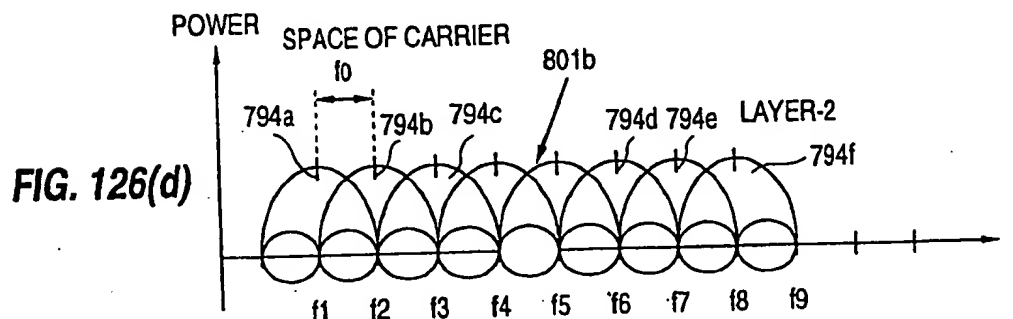
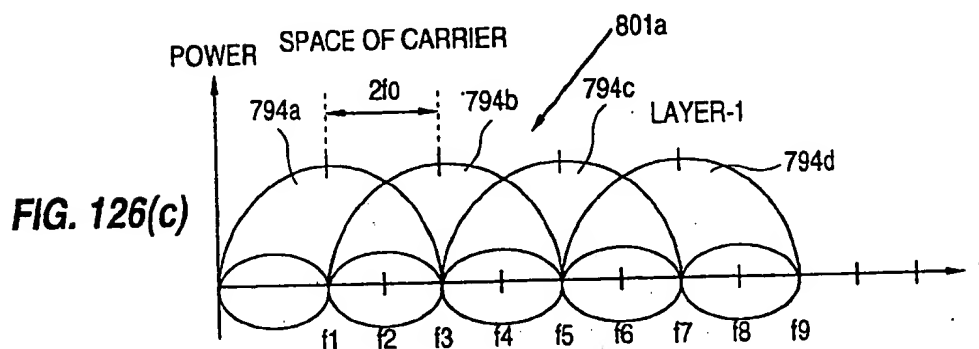
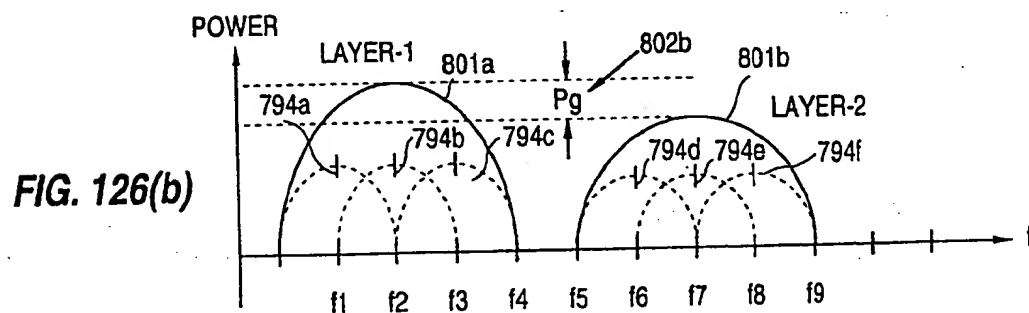
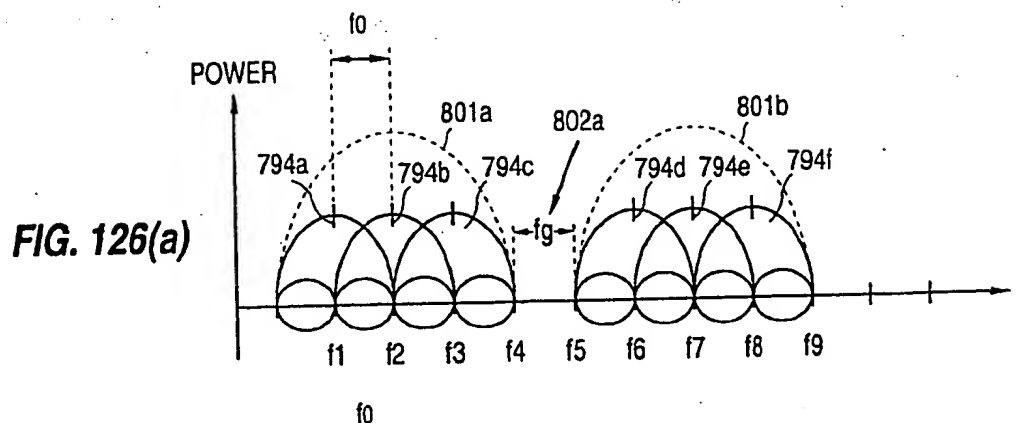


FIG. 127

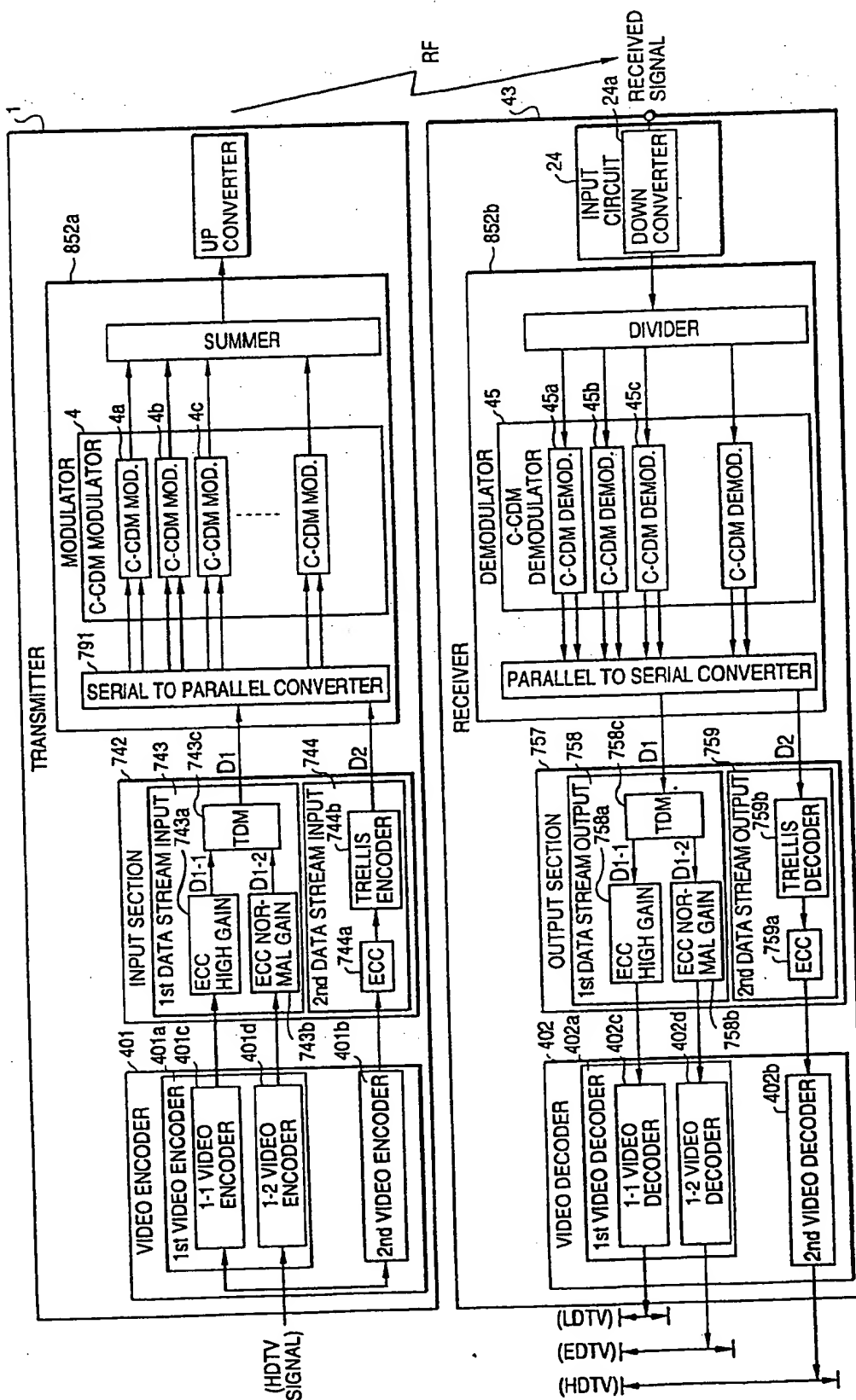


FIG. 128(a)

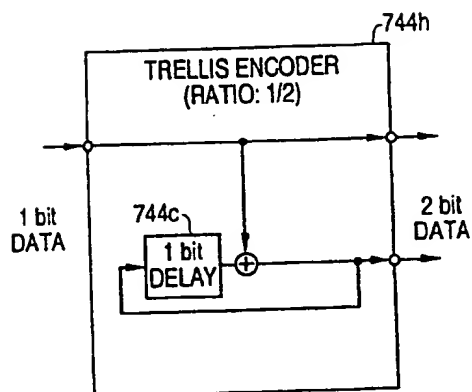


FIG. 128(d)

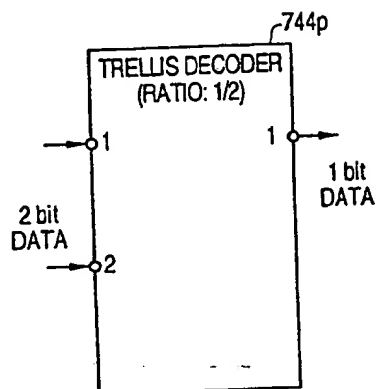


FIG. 128(b)

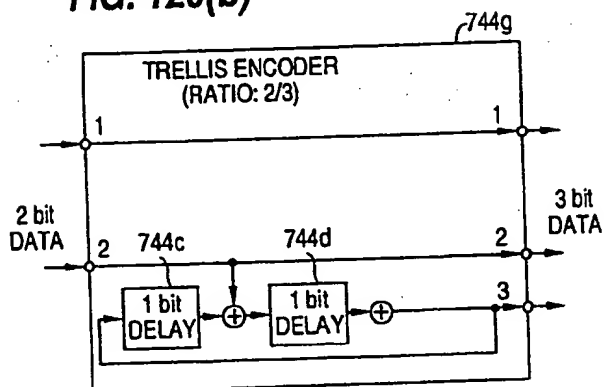


FIG. 128(e)

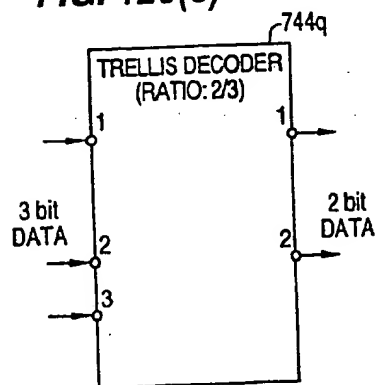


FIG. 128(c)

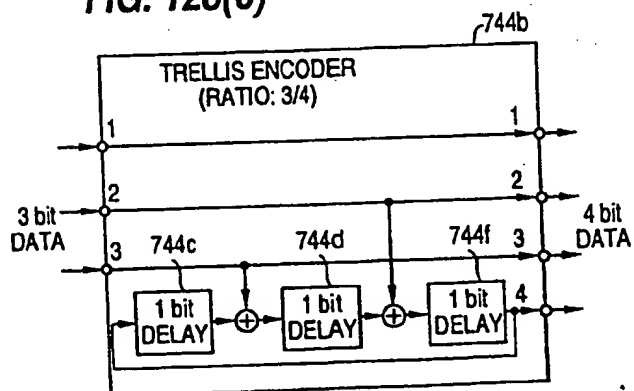


FIG. 128(f)

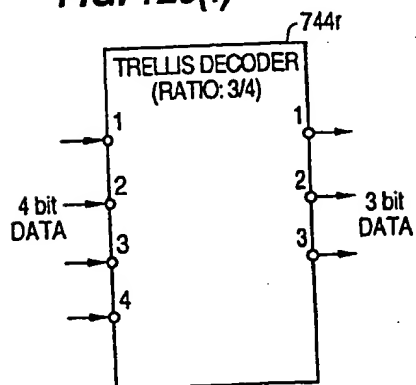


FIG. 129

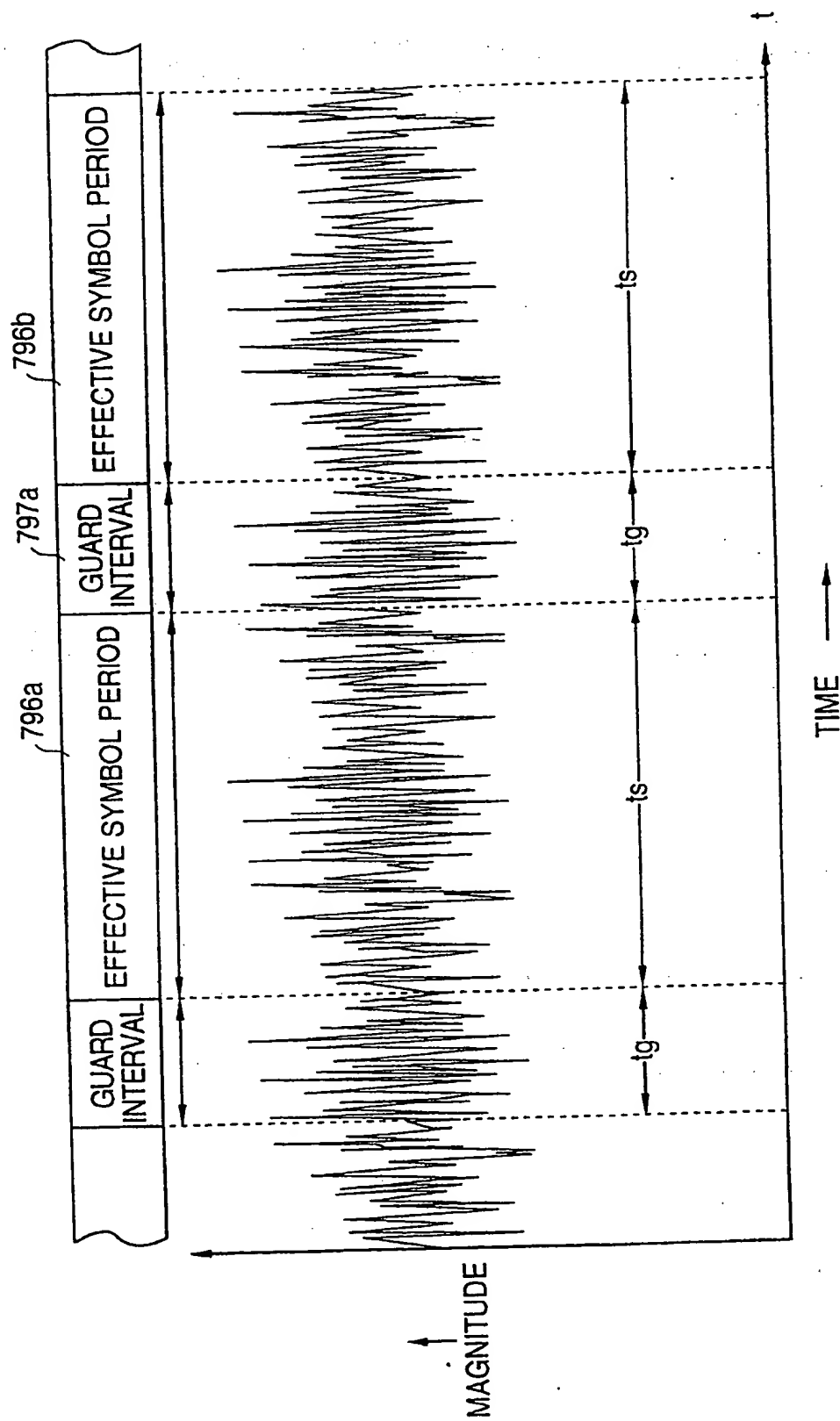


FIG. 130

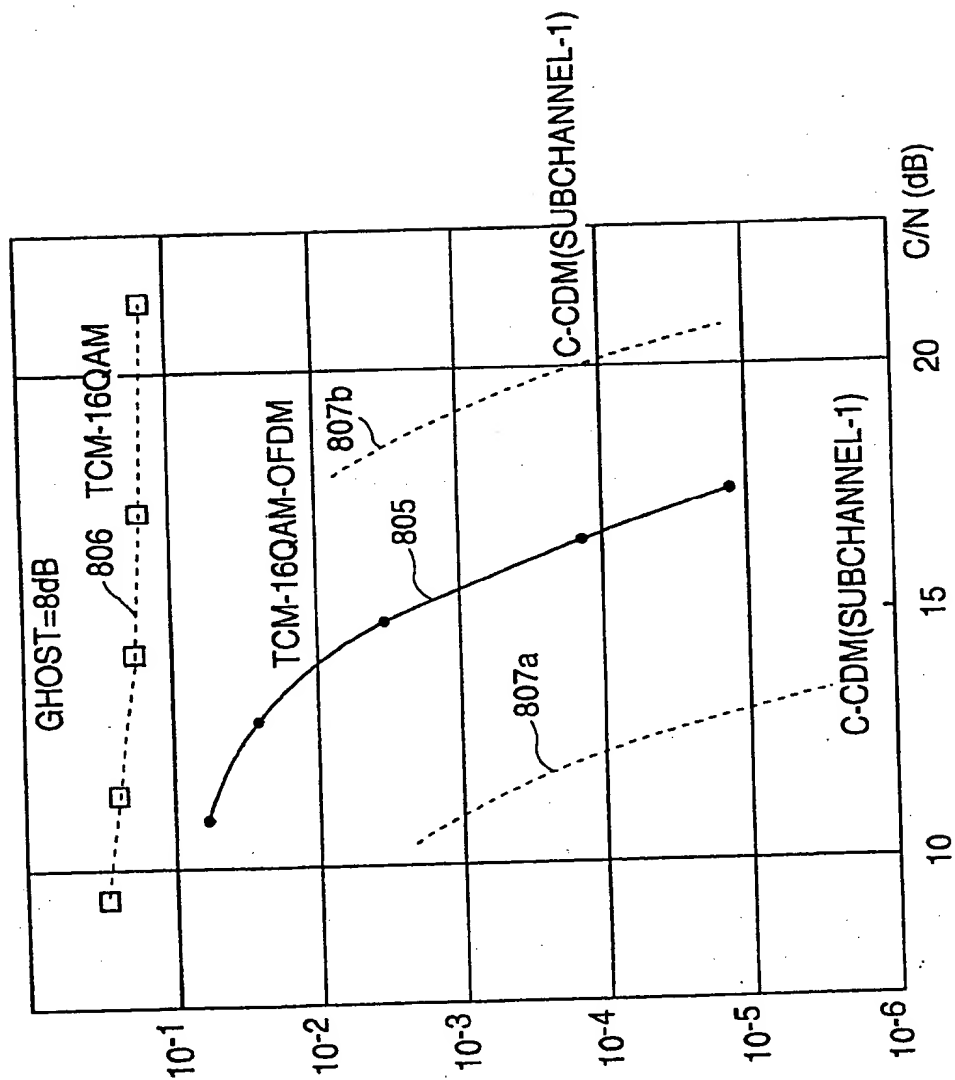


FIG. 131

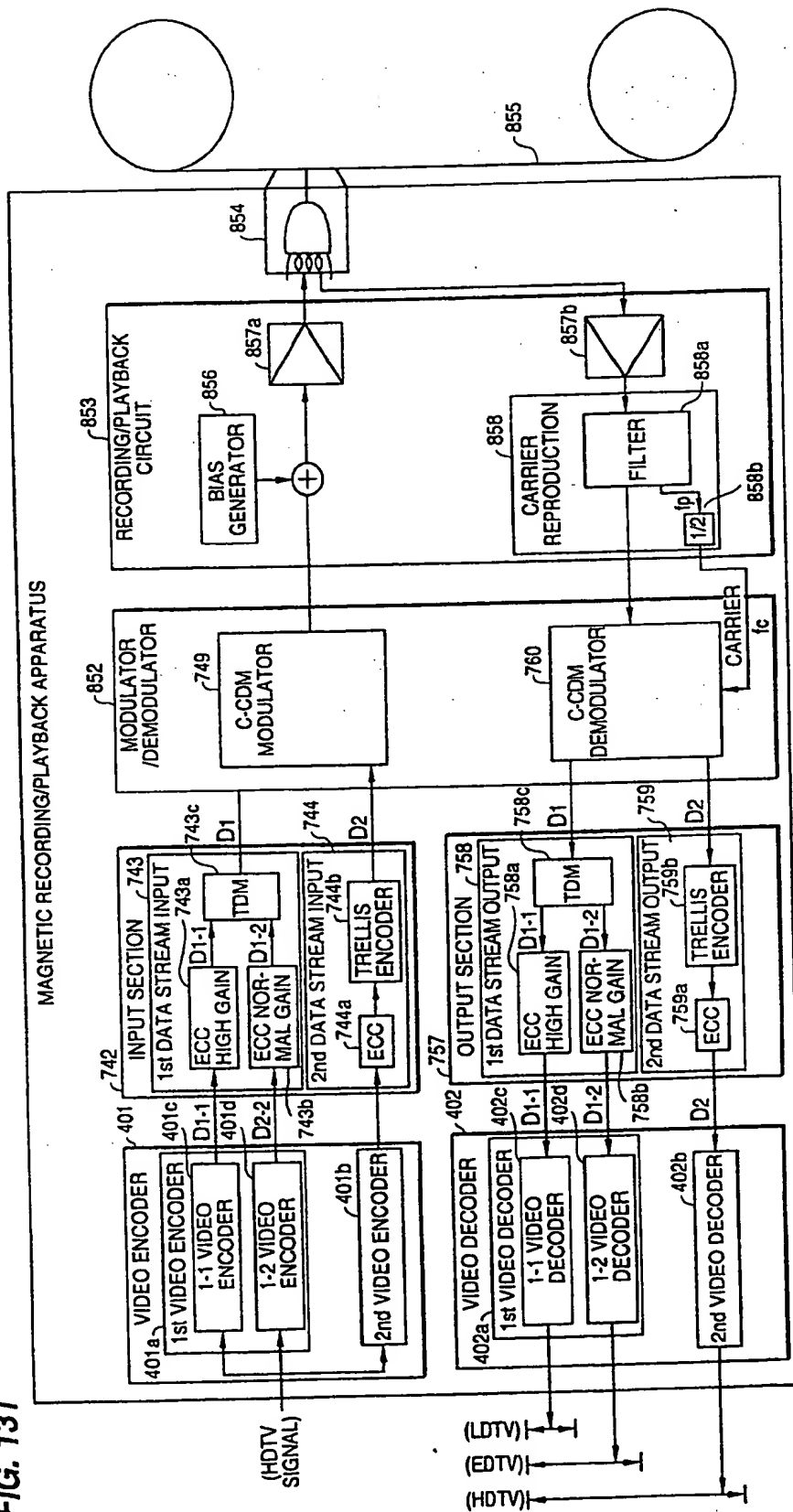


FIG. 132

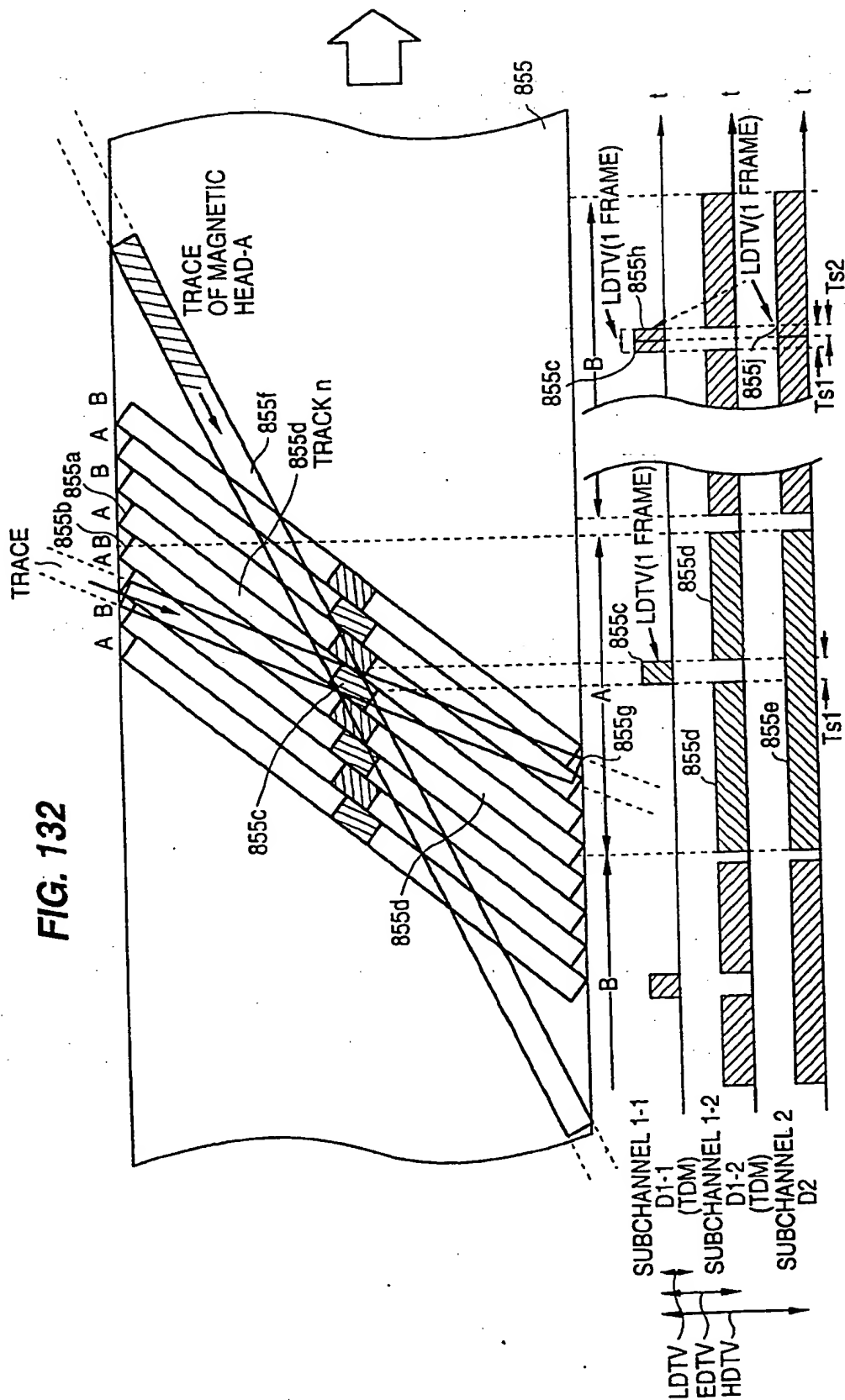


FIG. 133

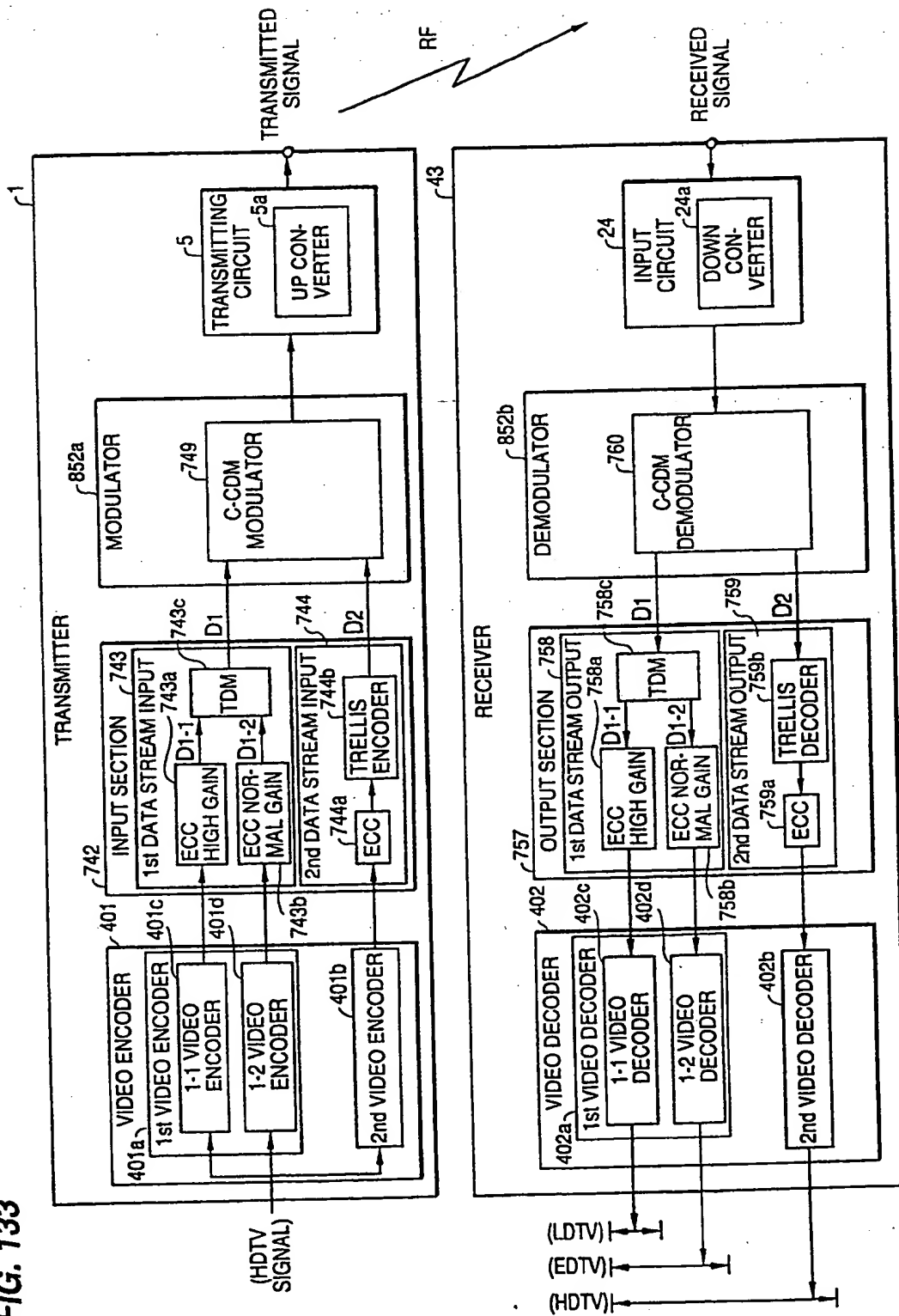


FIG. 134

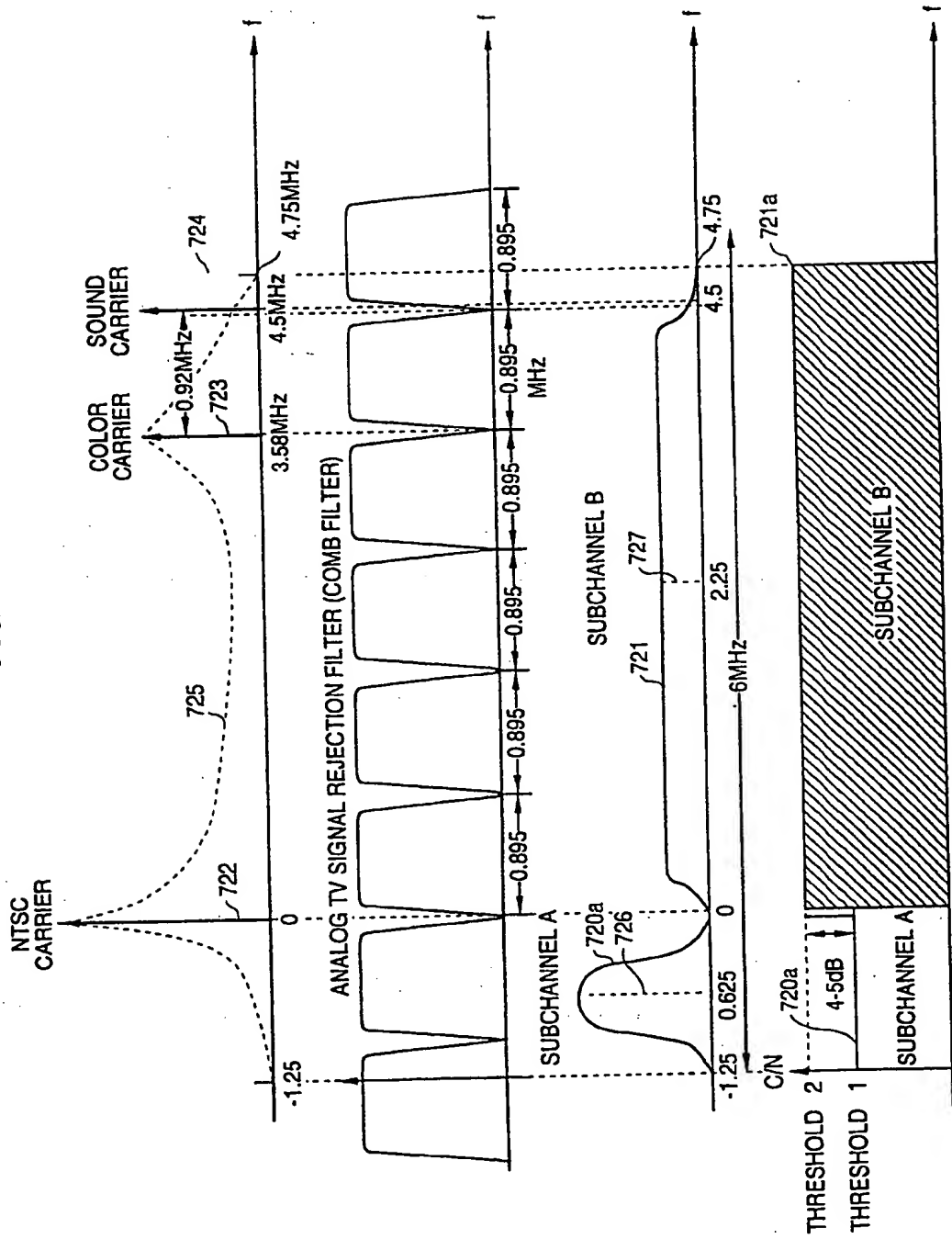


FIG. 135

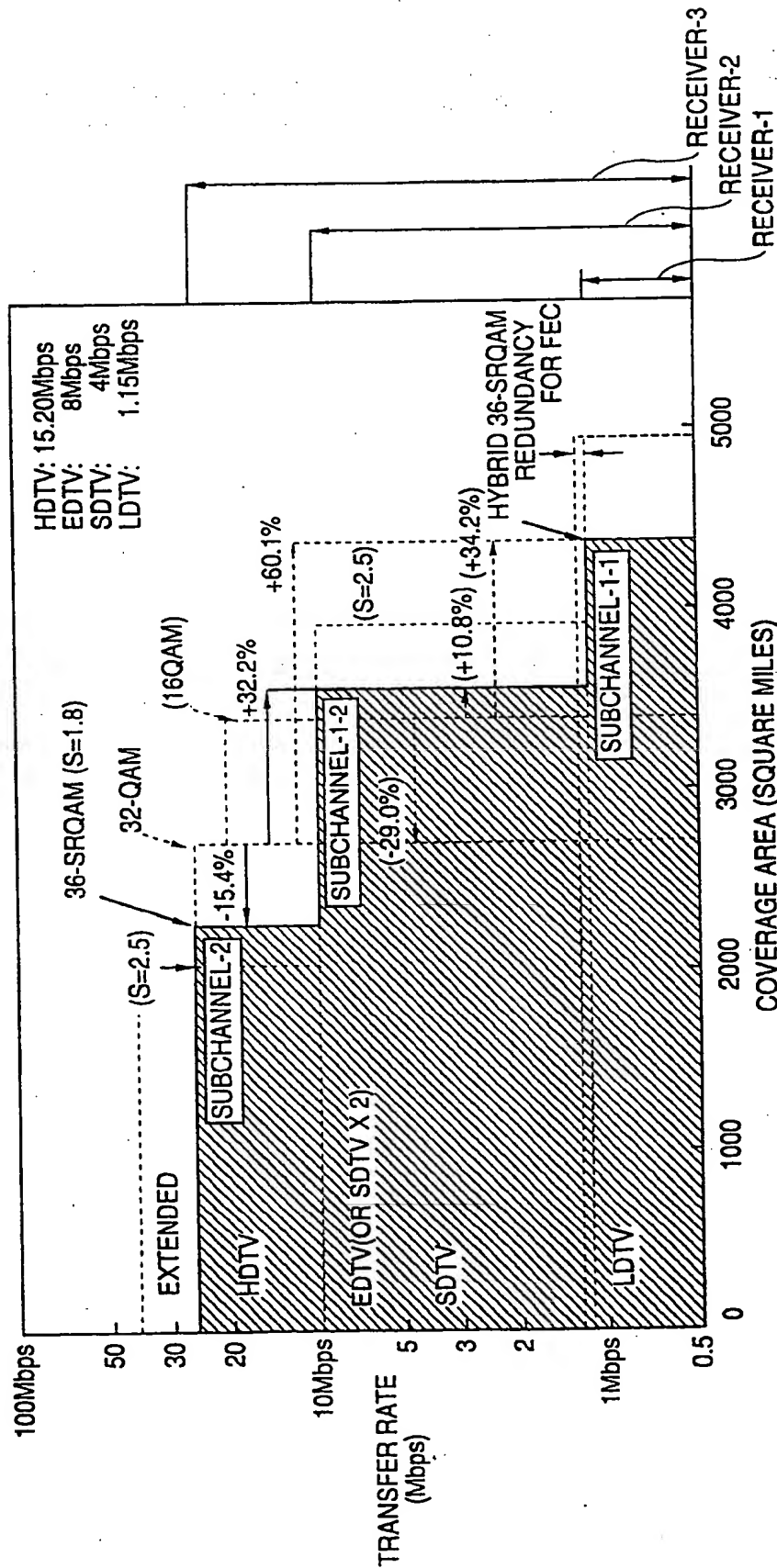


FIG. 136

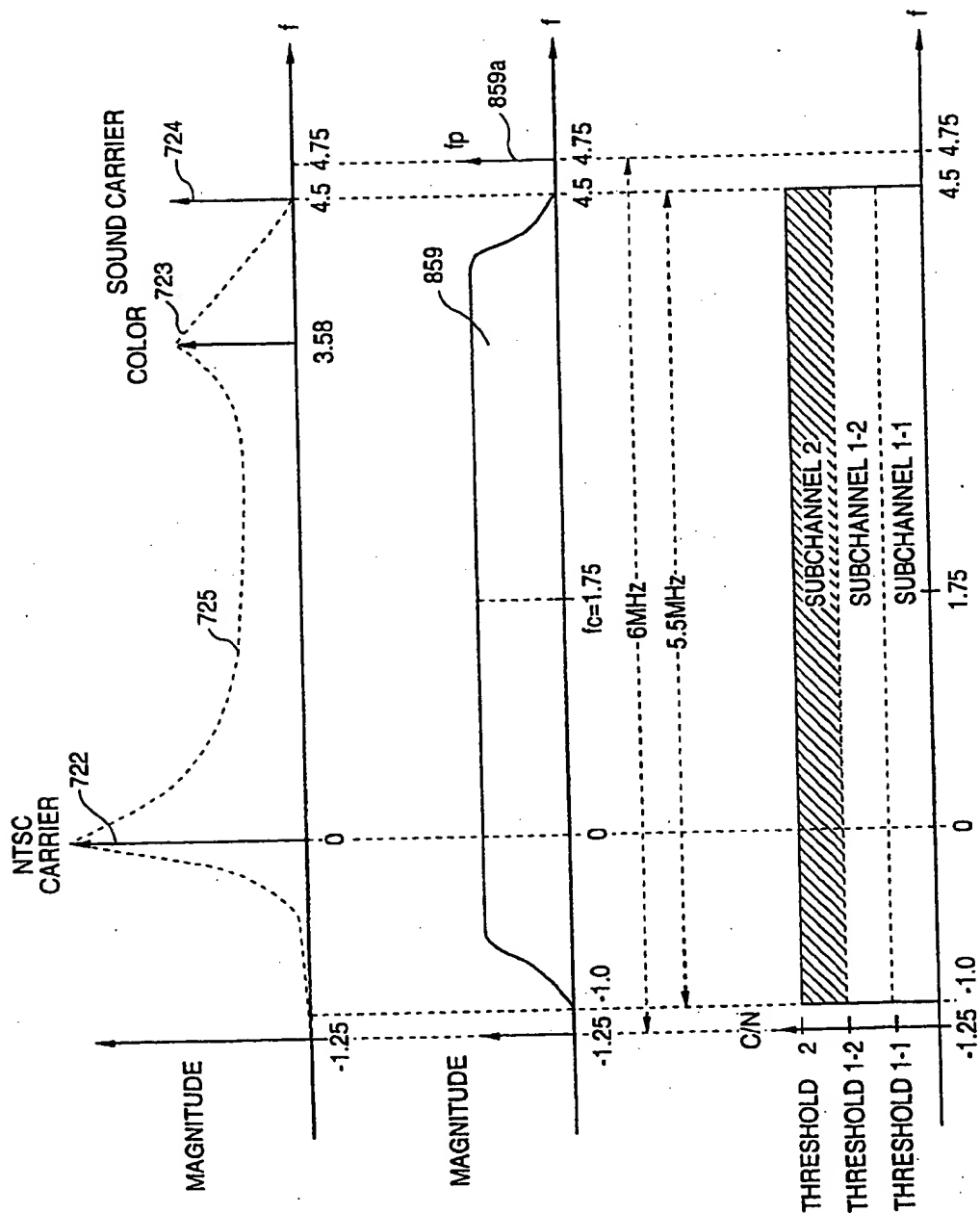


FIG. 137

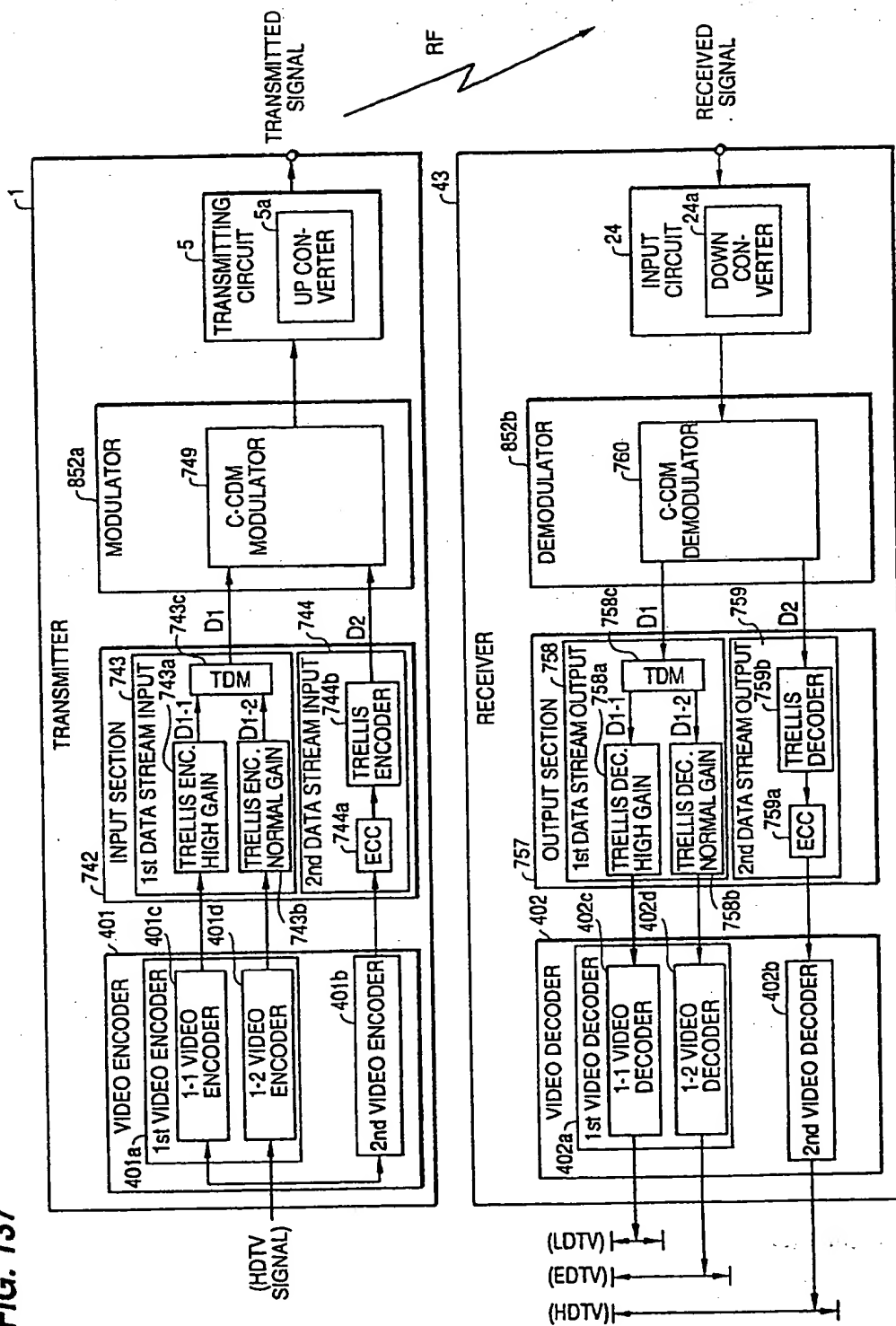


FIG. 138

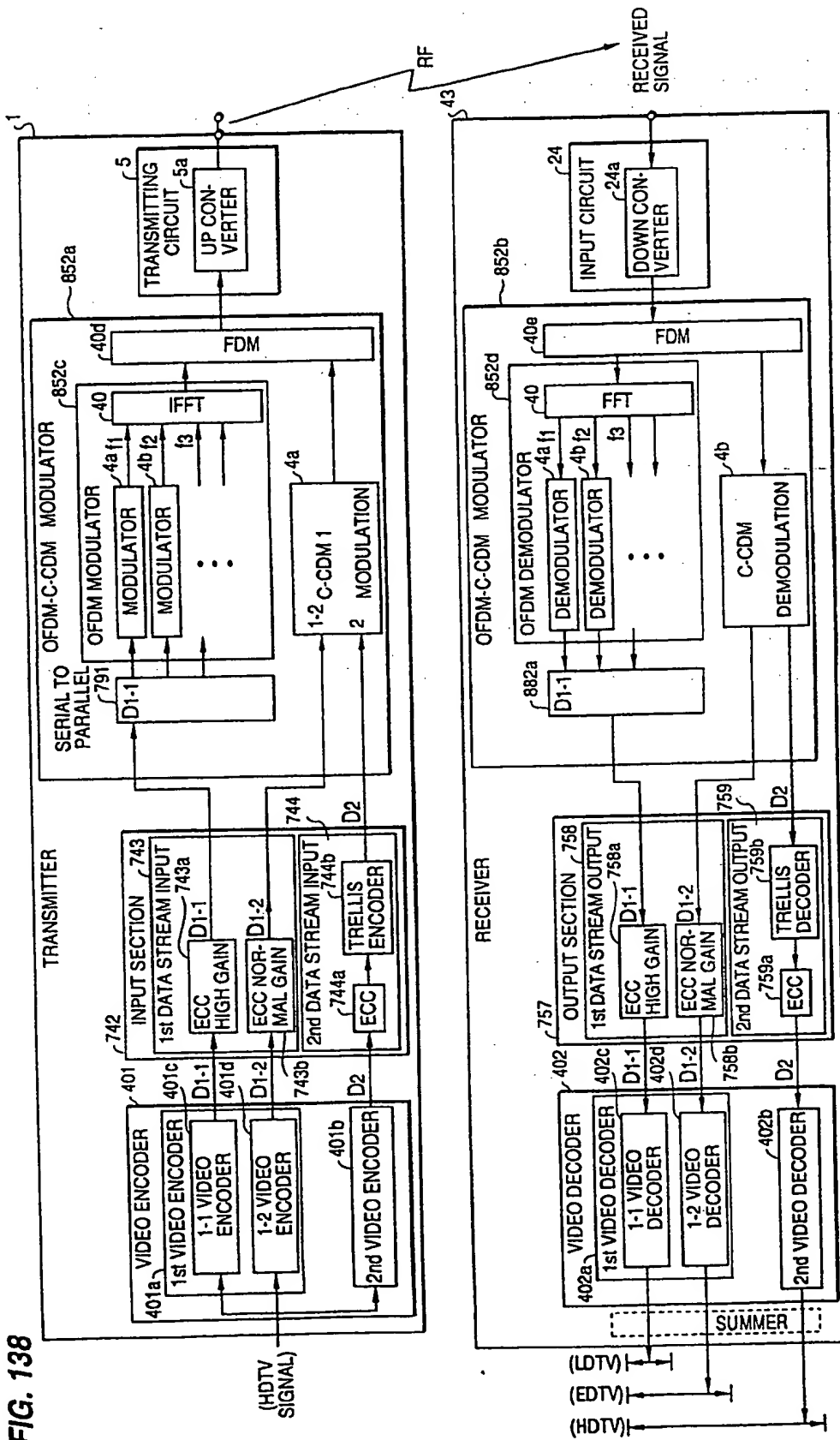


FIG. 139

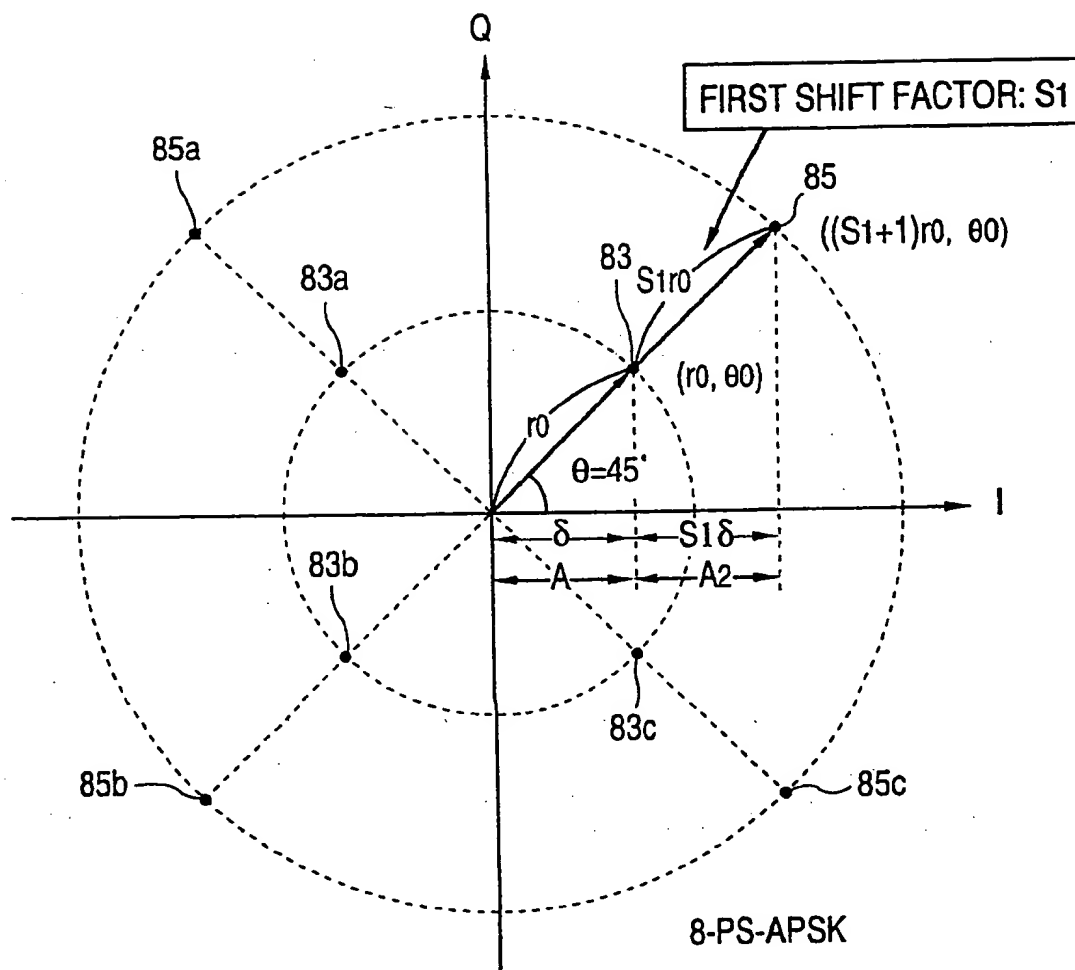


FIG. 140

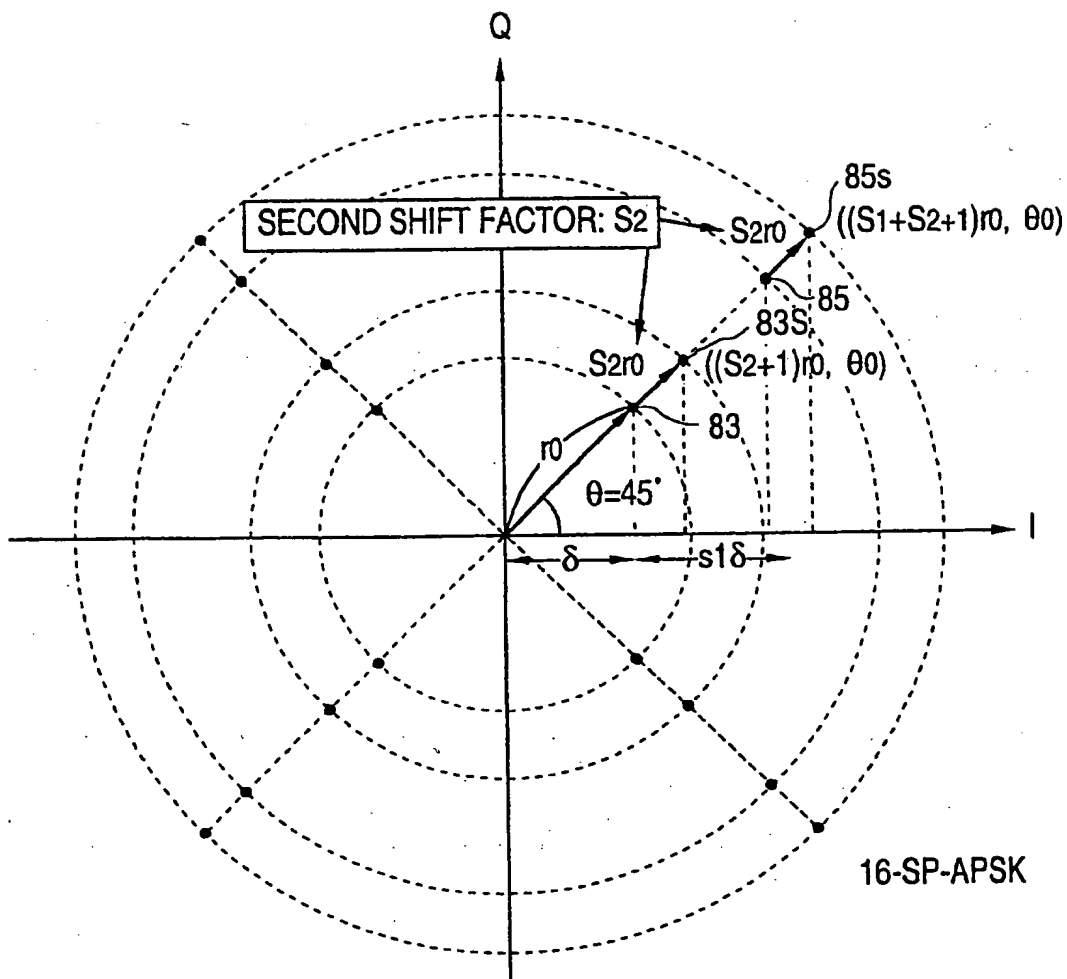


FIG. 141

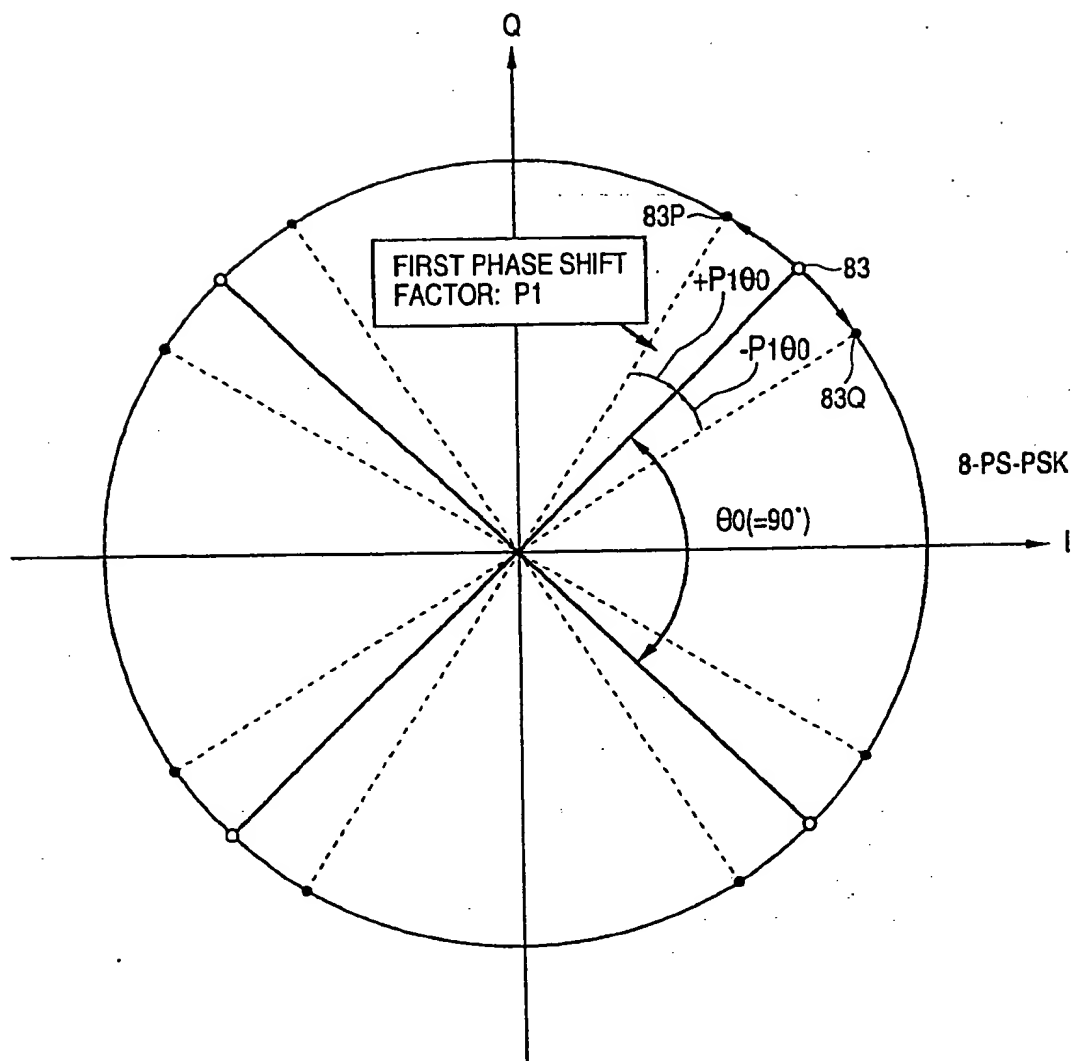


FIG. 142

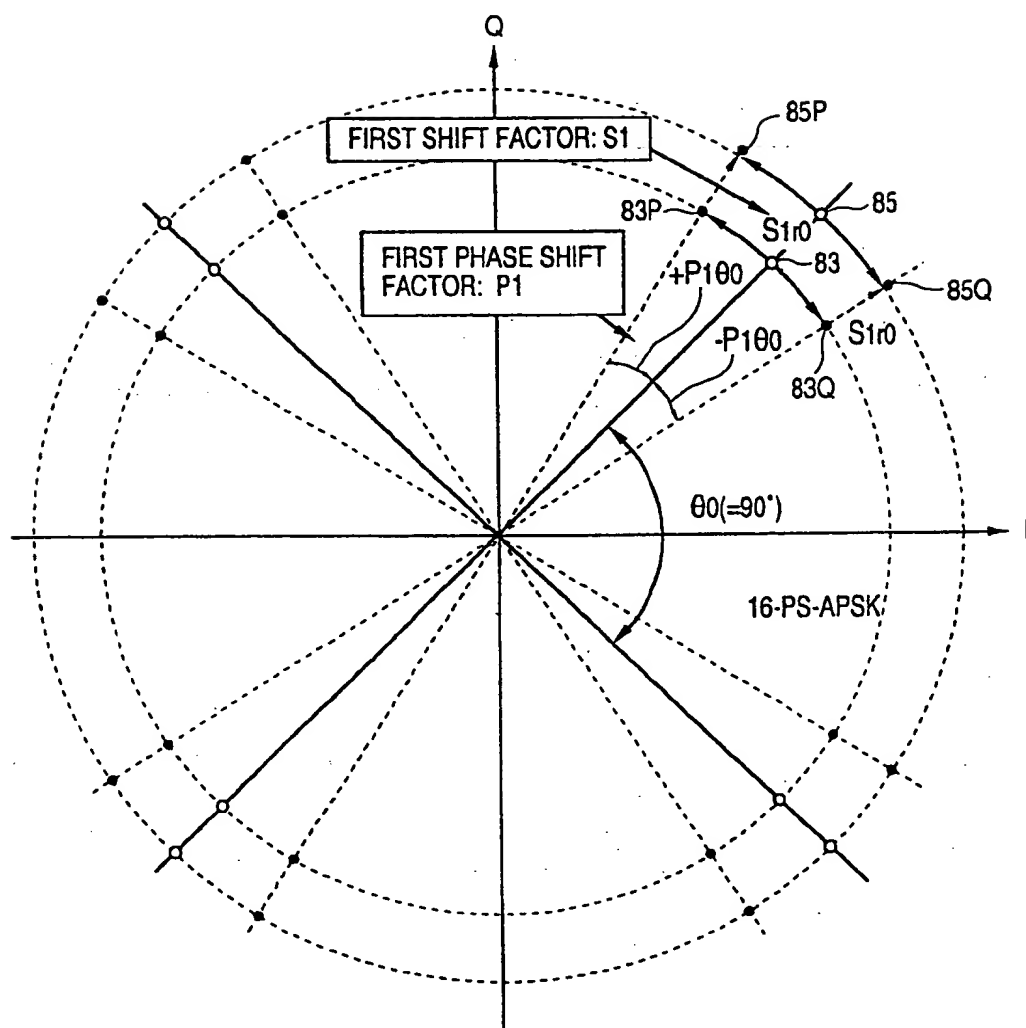


FIG. 143

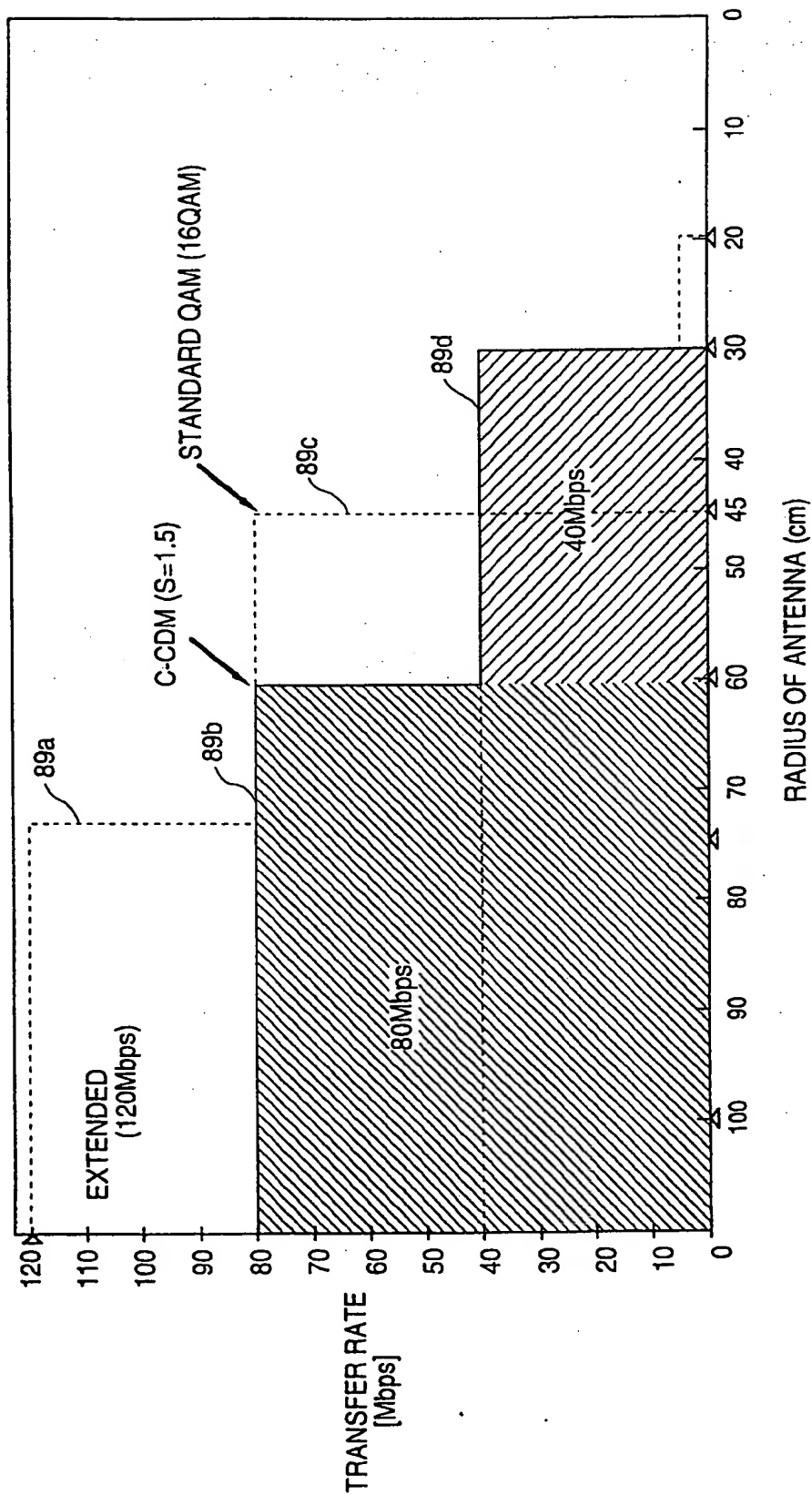
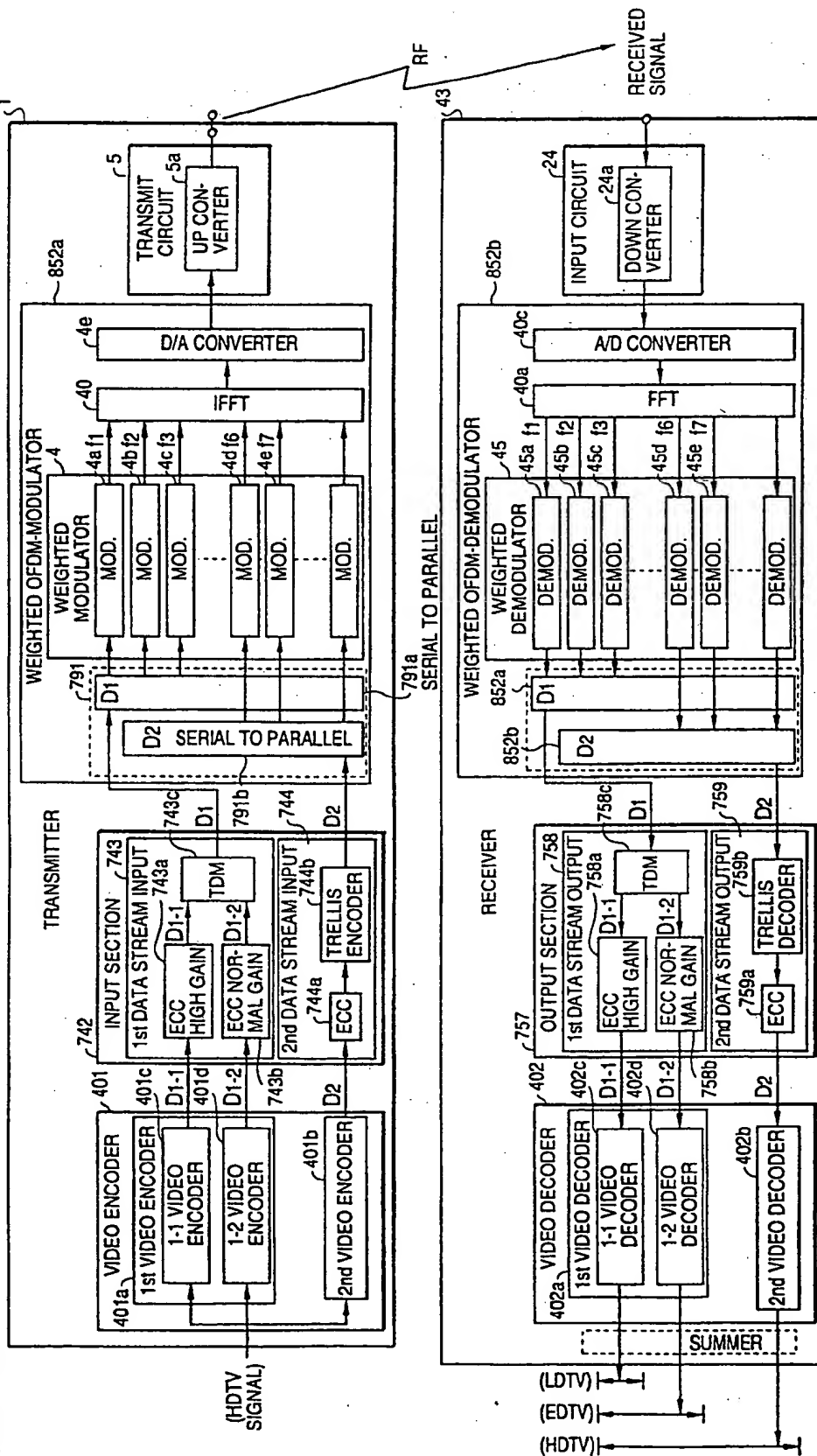


FIG. 144



Timing diagram for a four-bit shift register. The diagram shows four clock cycles labeled 811a, 811b, 811c, and 811d. Each cycle has a setup time (tsa or tsb) and a hold time (tga or tgb). The data input is 'A' and the data output is 'B'. The output 'B' is shown as a series of pulses that shift right by one bit in each clock cycle.

FIG. 146

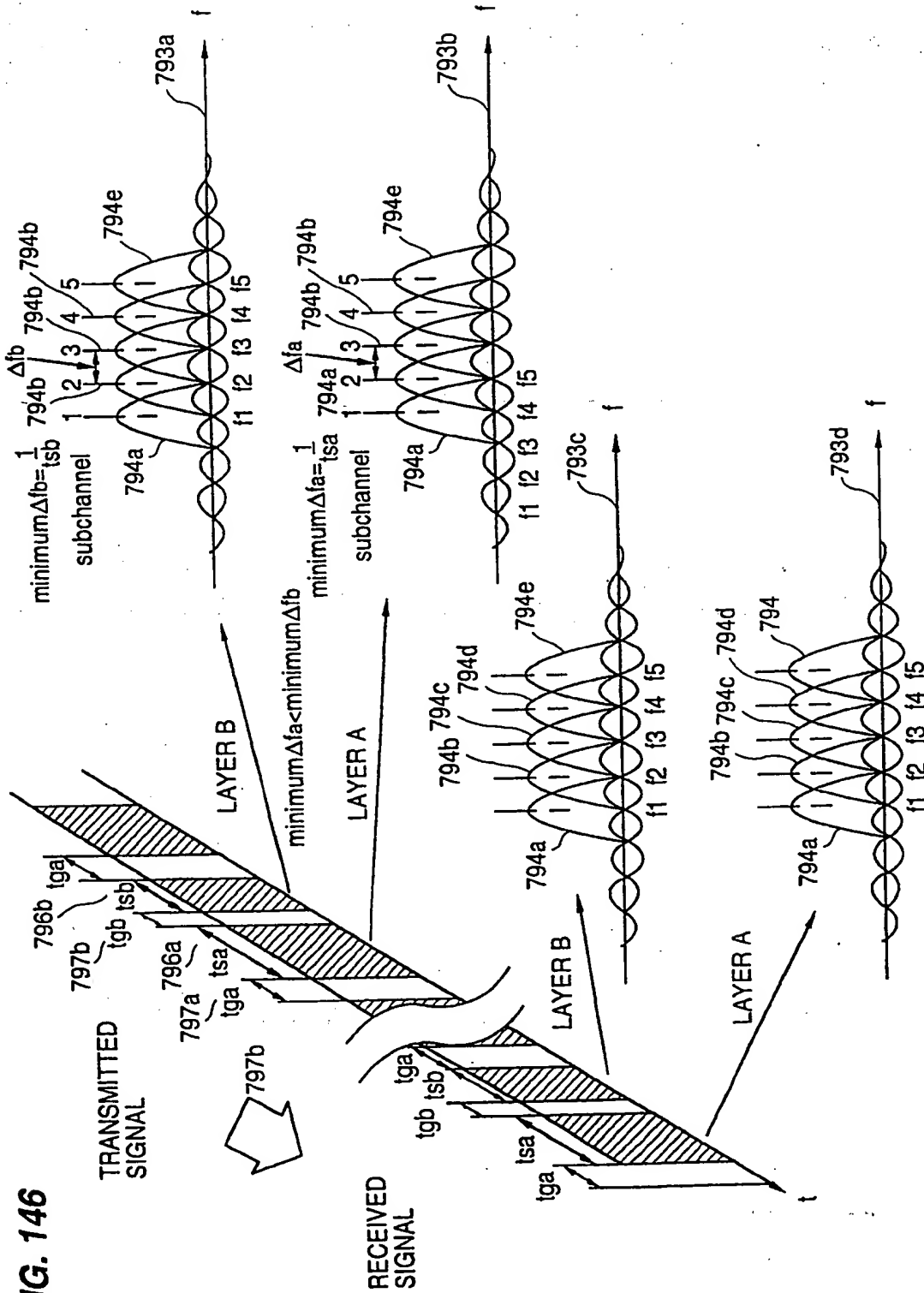


FIG. 147

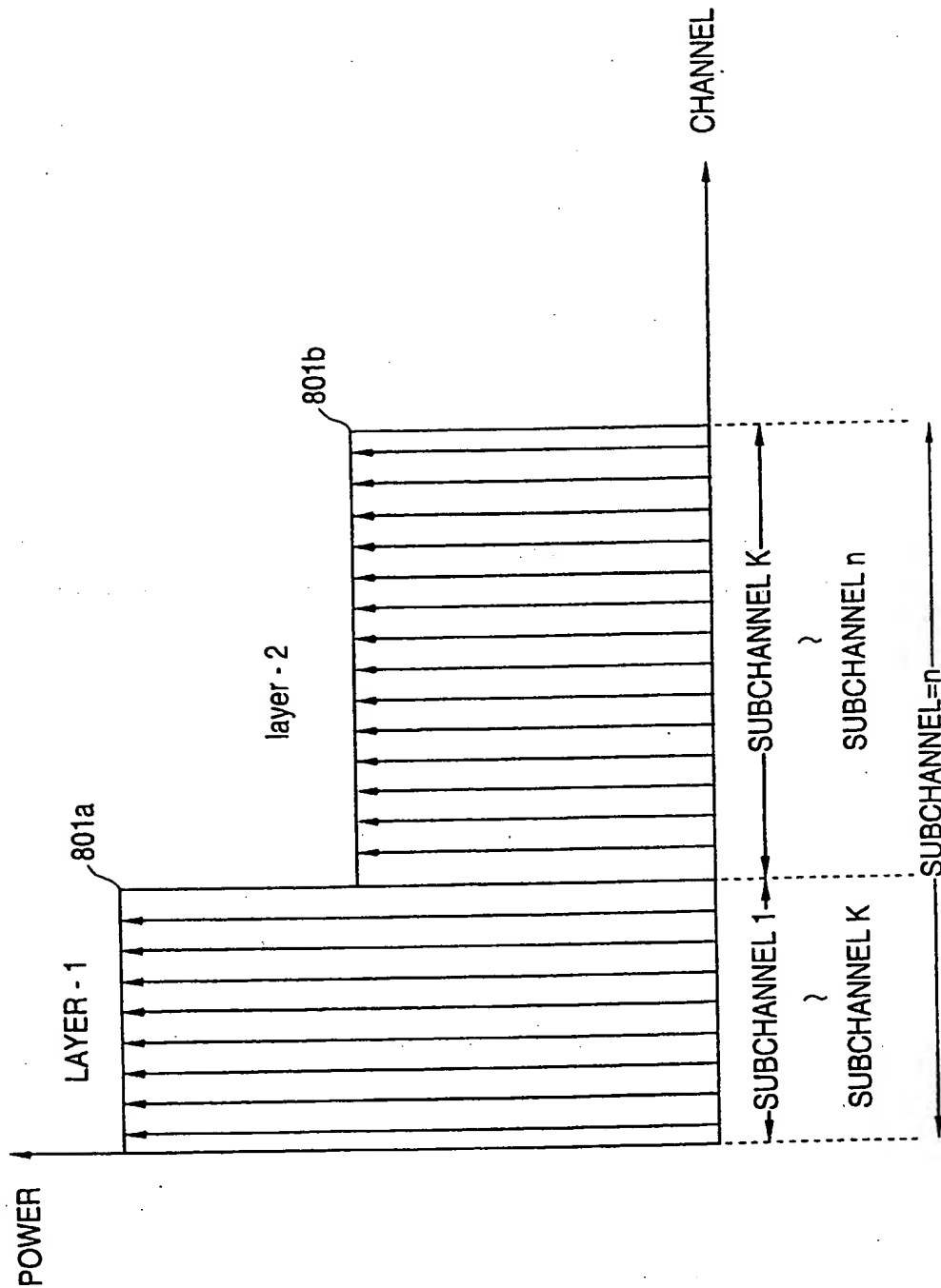


FIG. 148

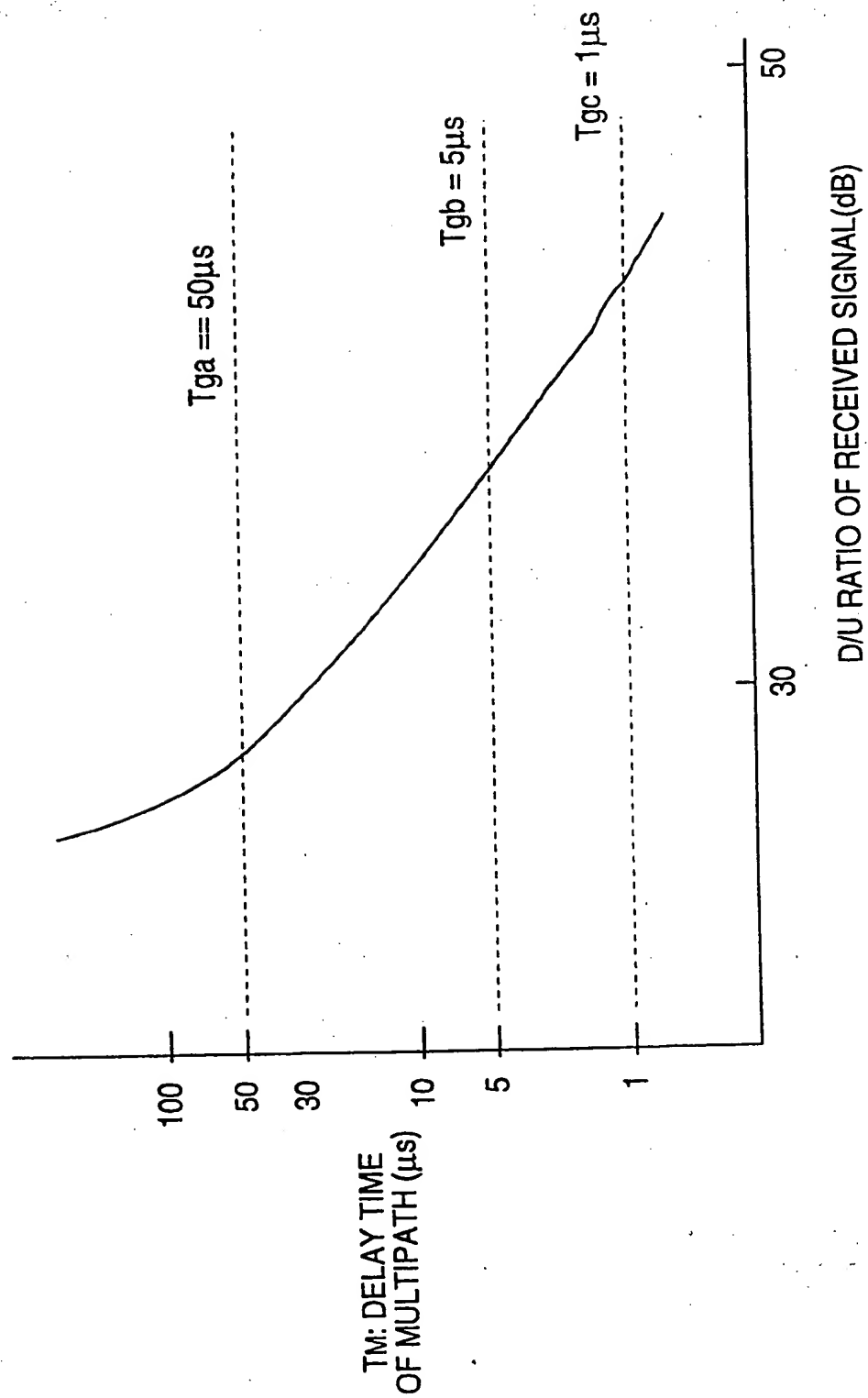


FIG. 149(a)

FIG. 150

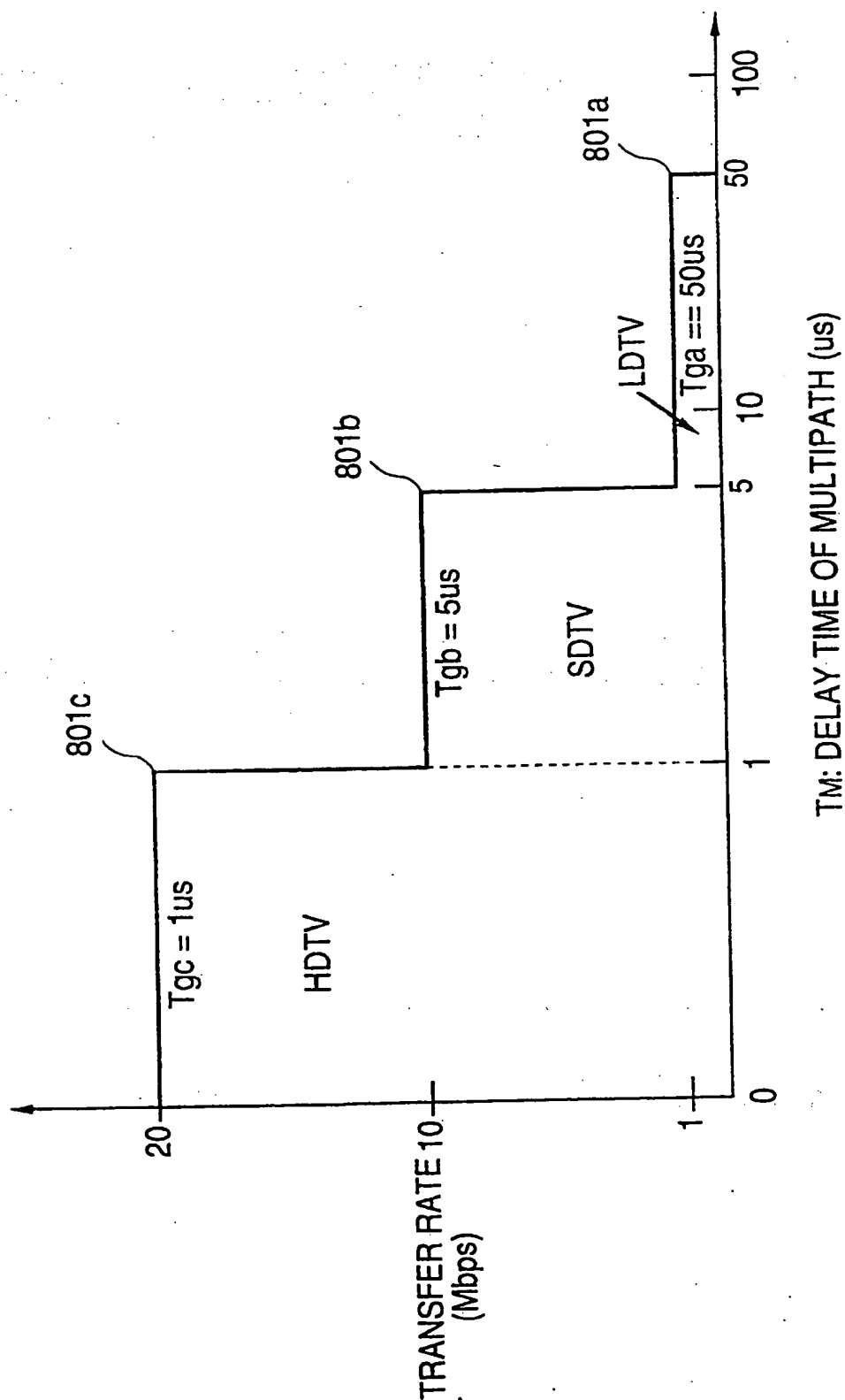


FIG. 151

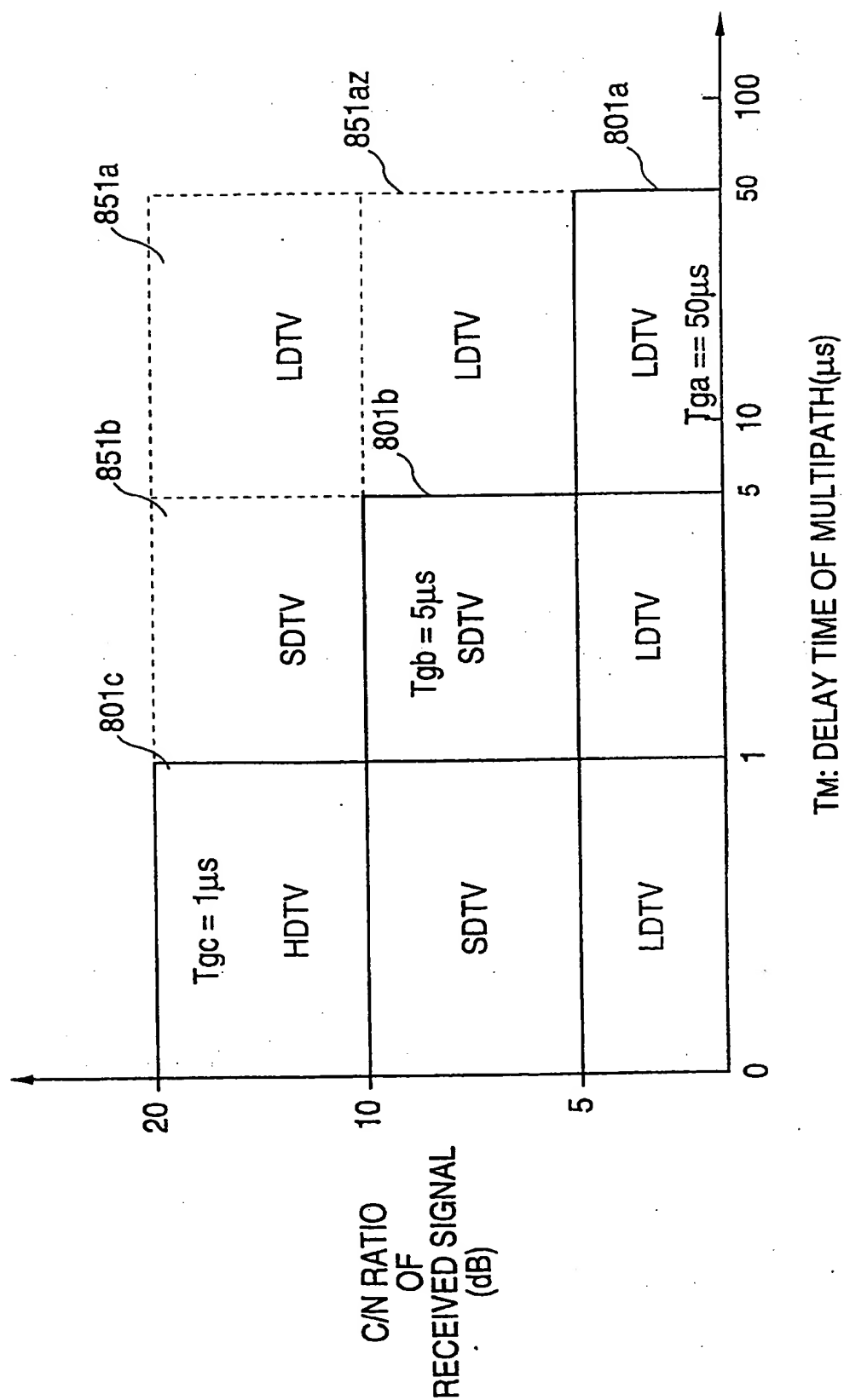


FIG. 152

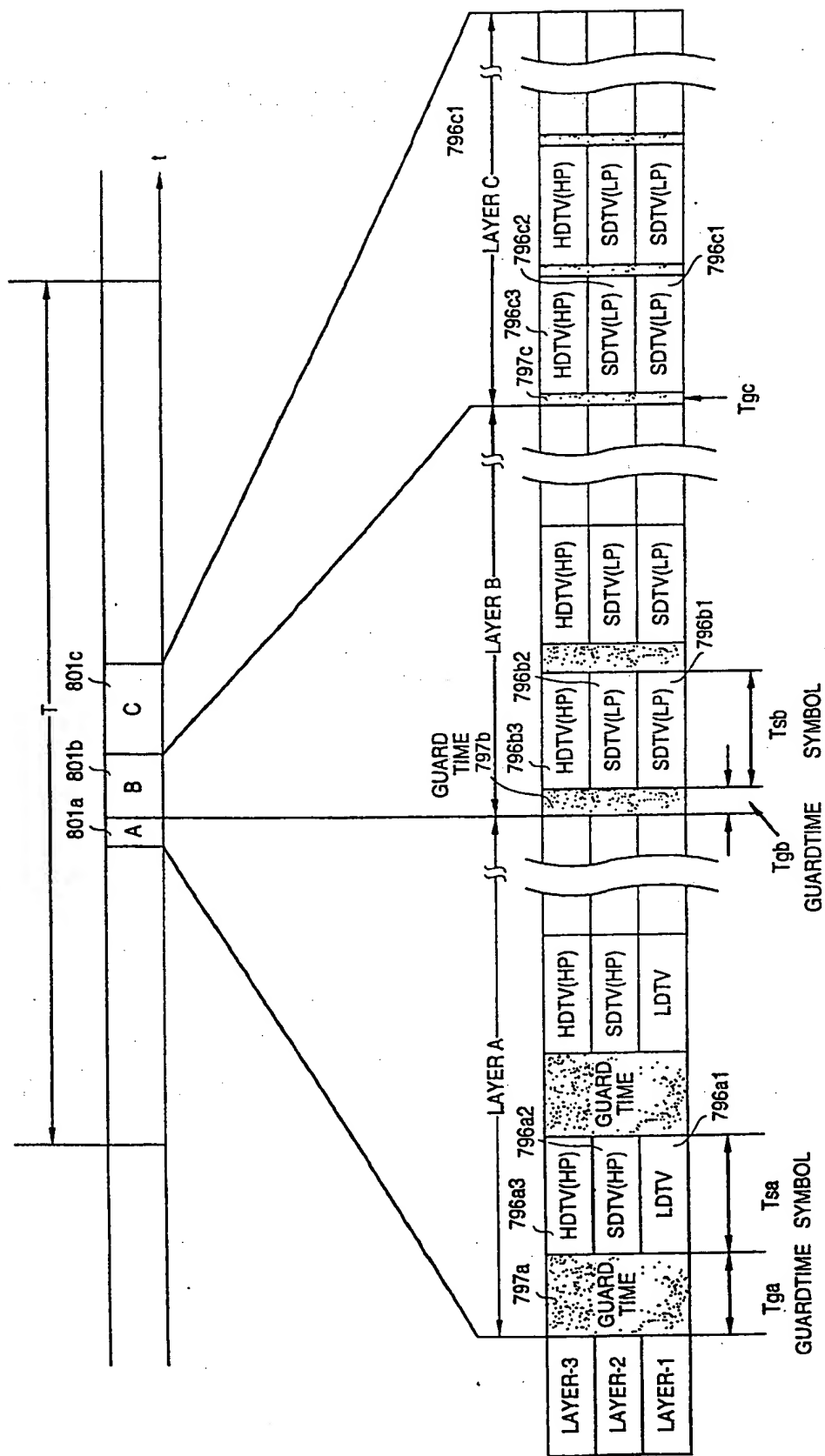


FIG. 153

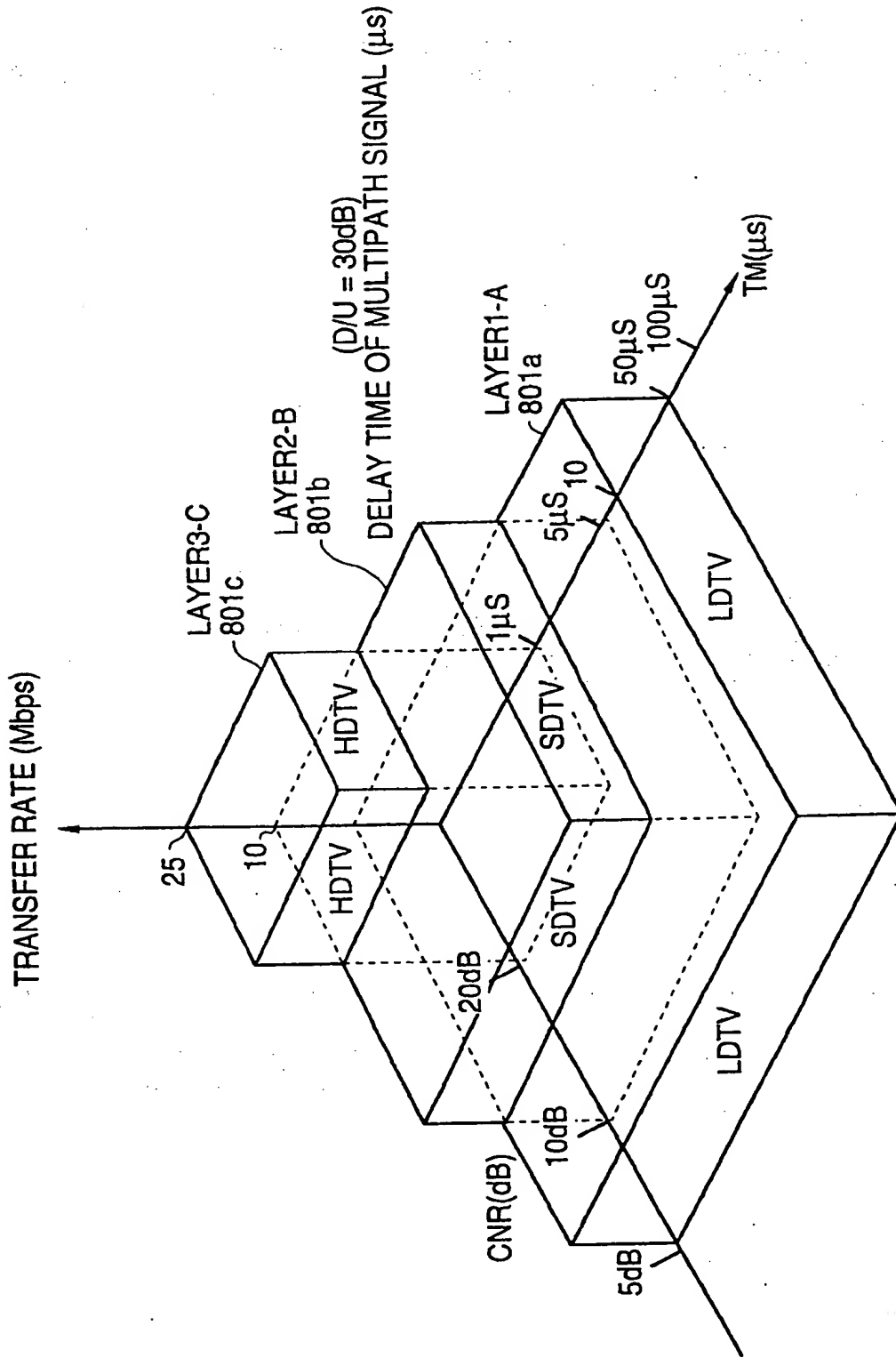


FIG. 154(a)

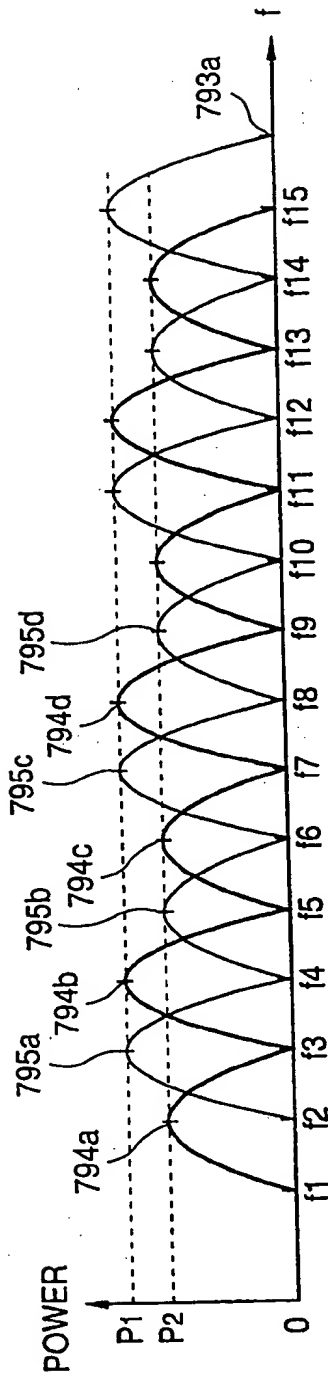


FIG. 154(b)

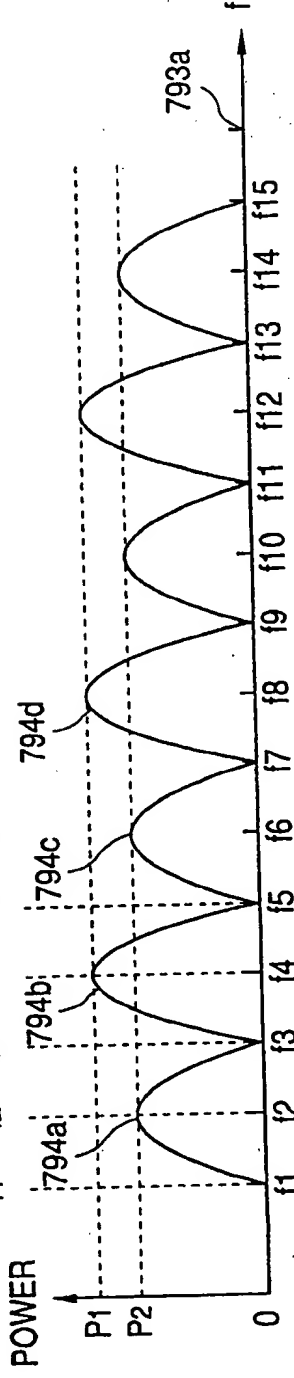


FIG. 154(c)

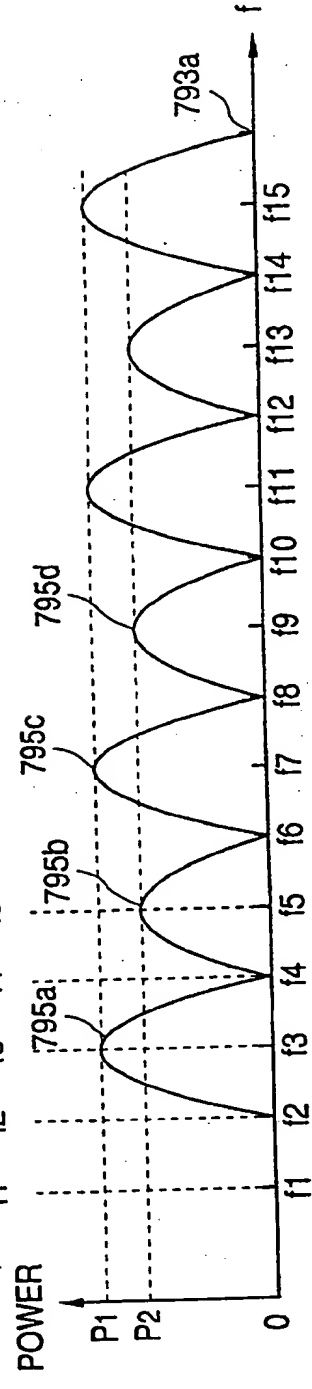


FIG. 155

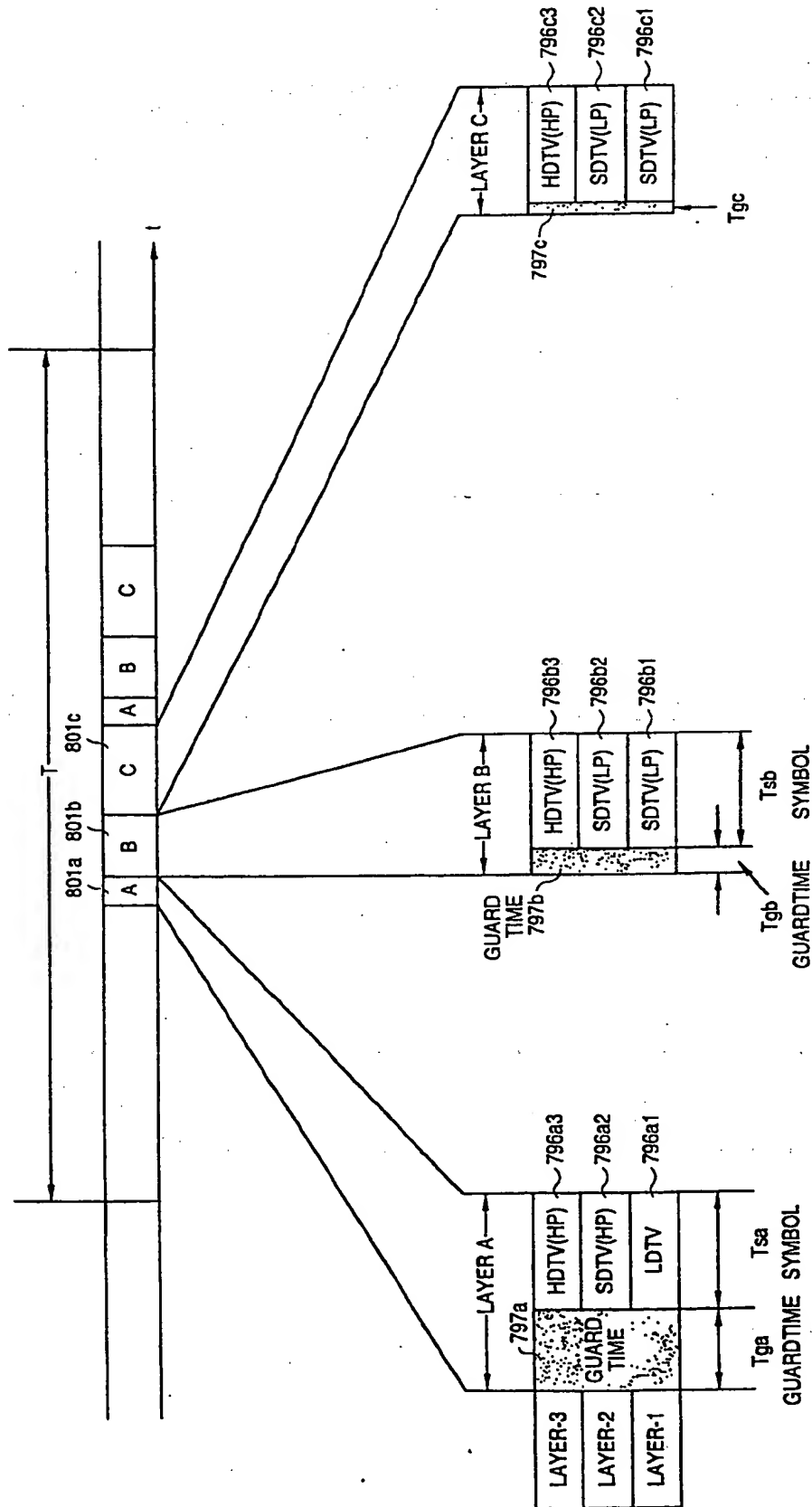


FIG. 156

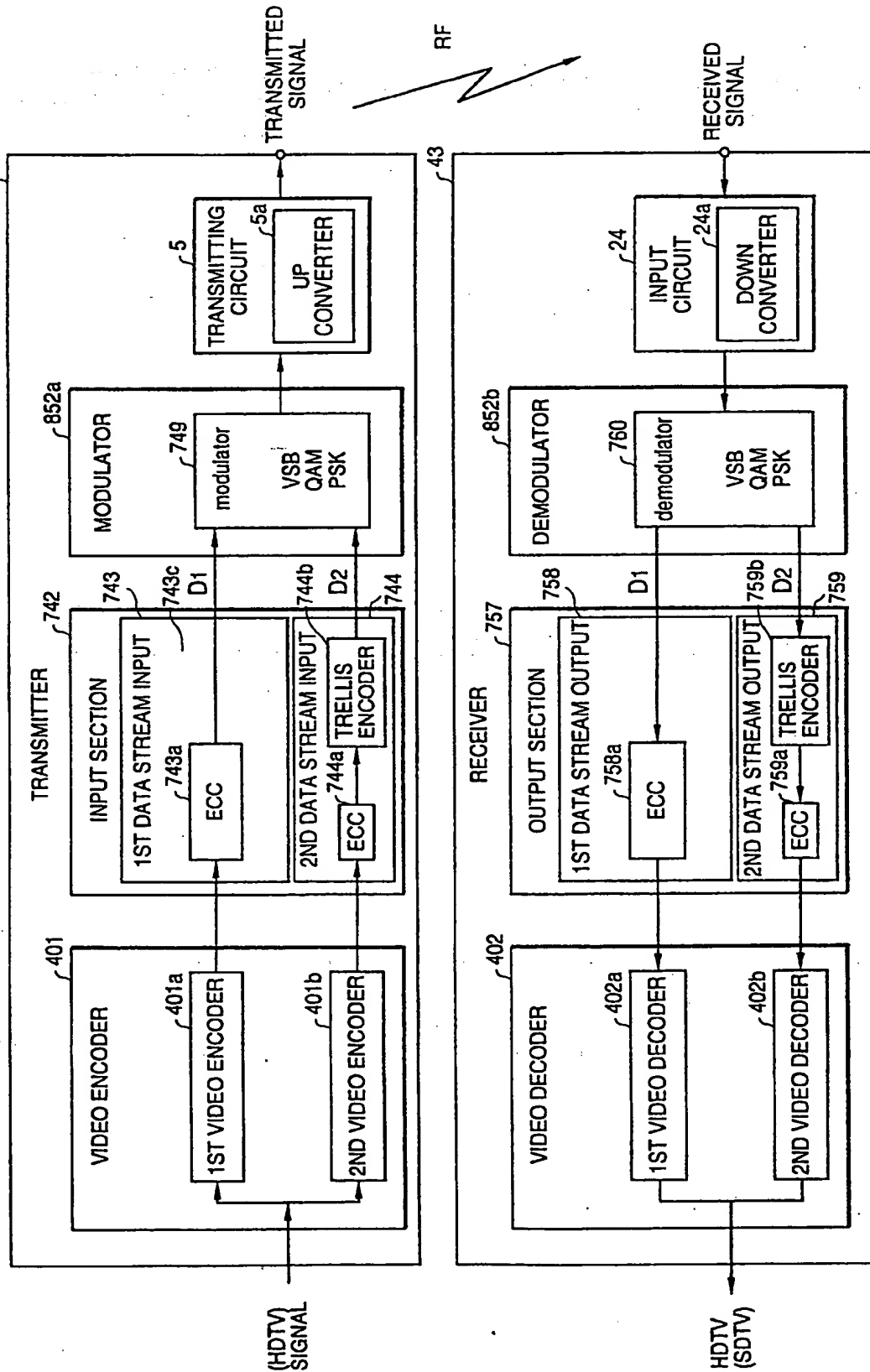


FIG. 157

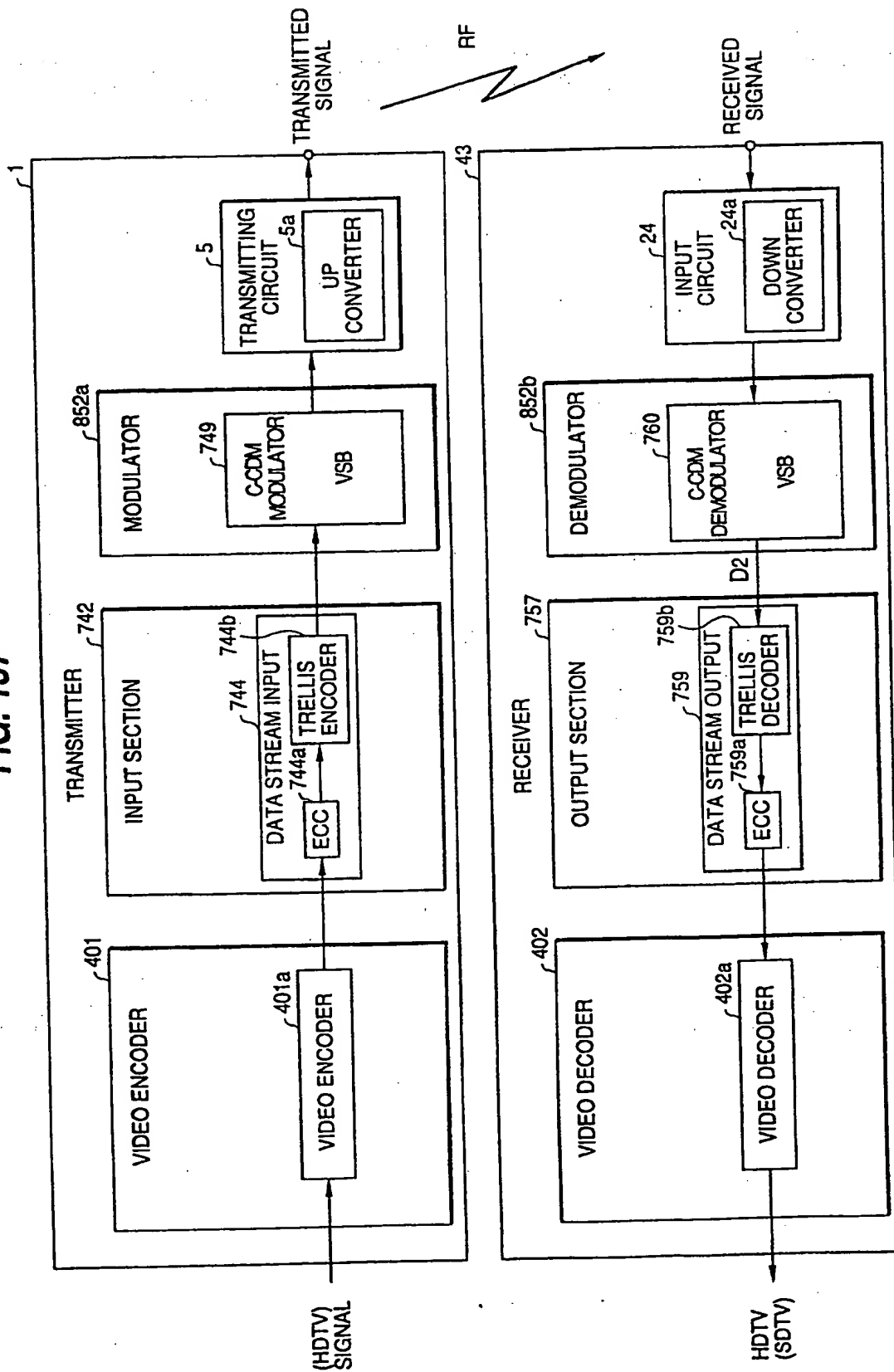
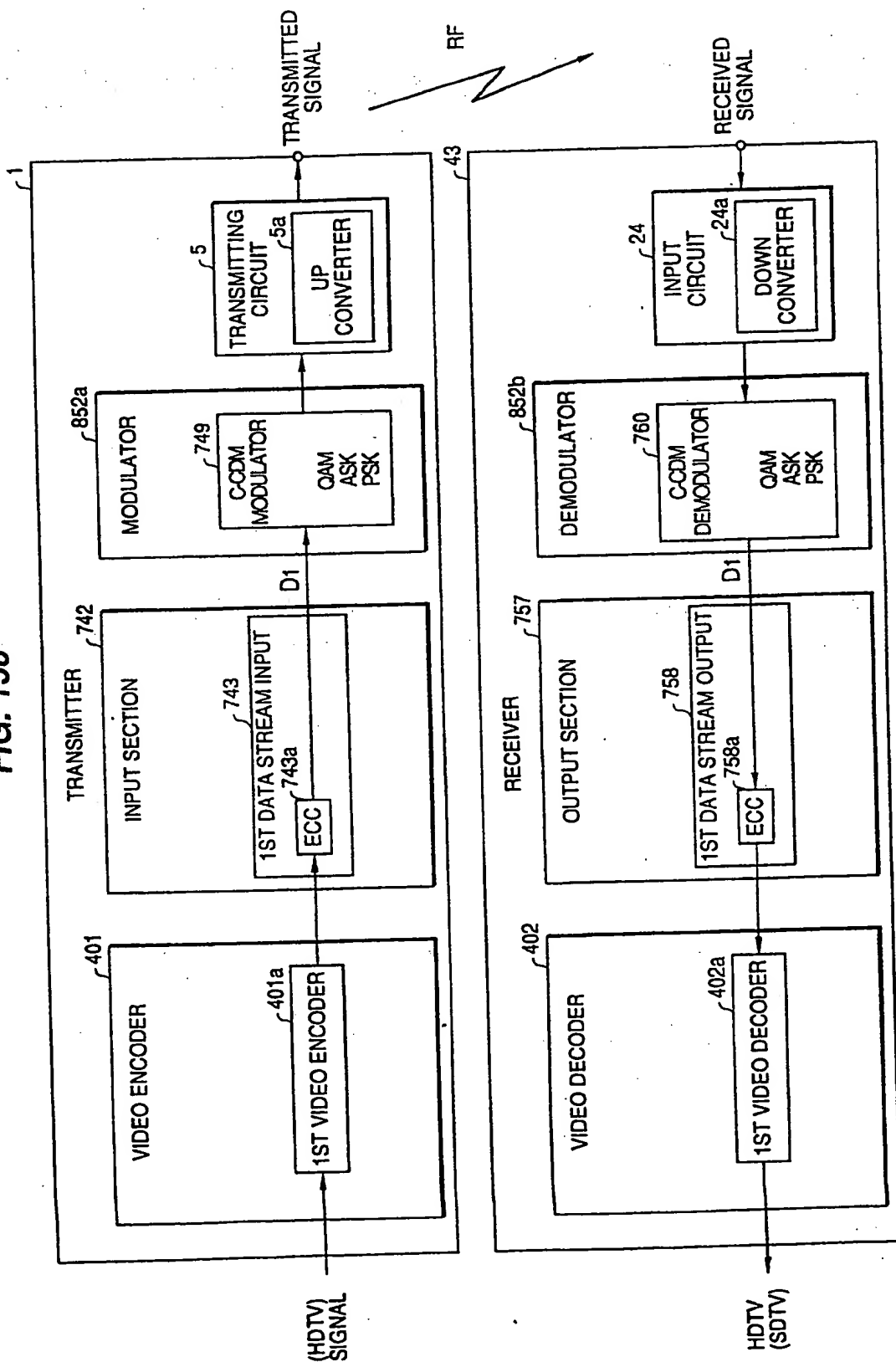


FIG. 158



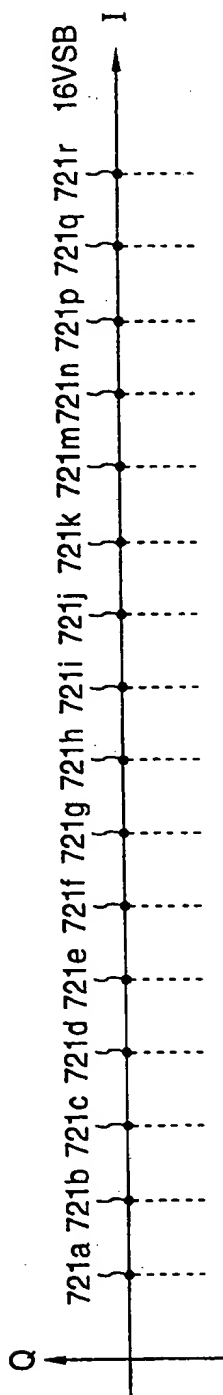


FIG. 159(a)

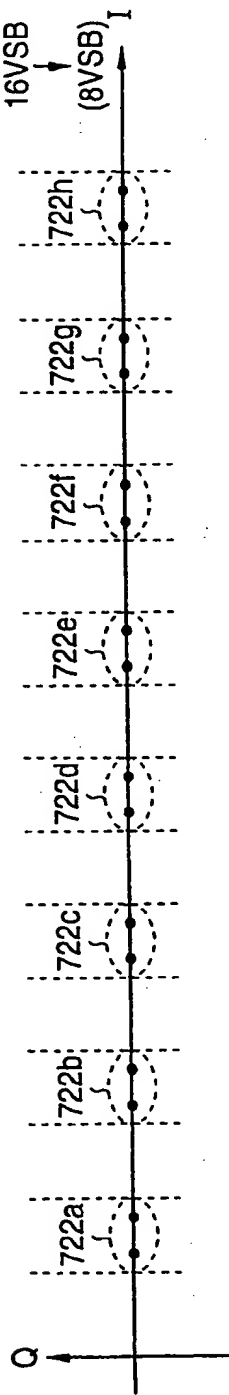


FIG. 159(b)

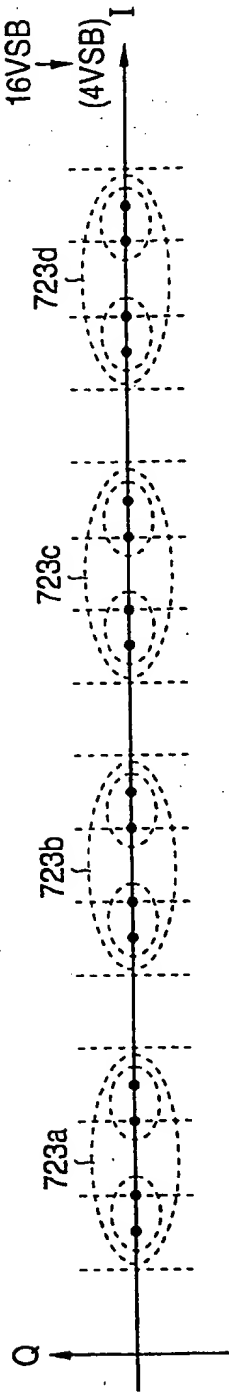


FIG. 159(c)

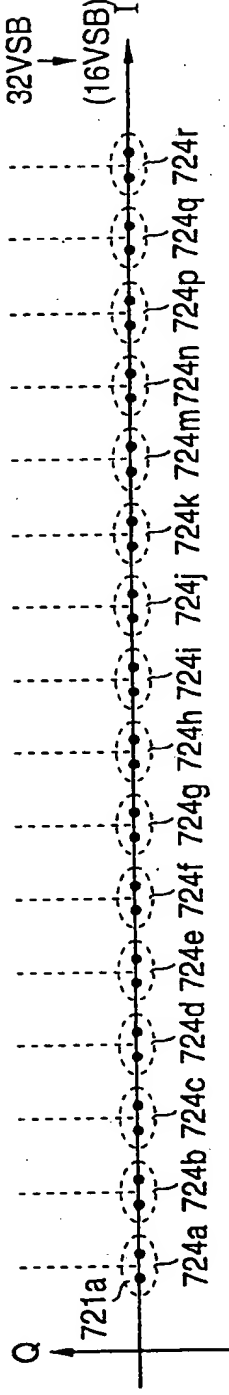


FIG. 159(d)

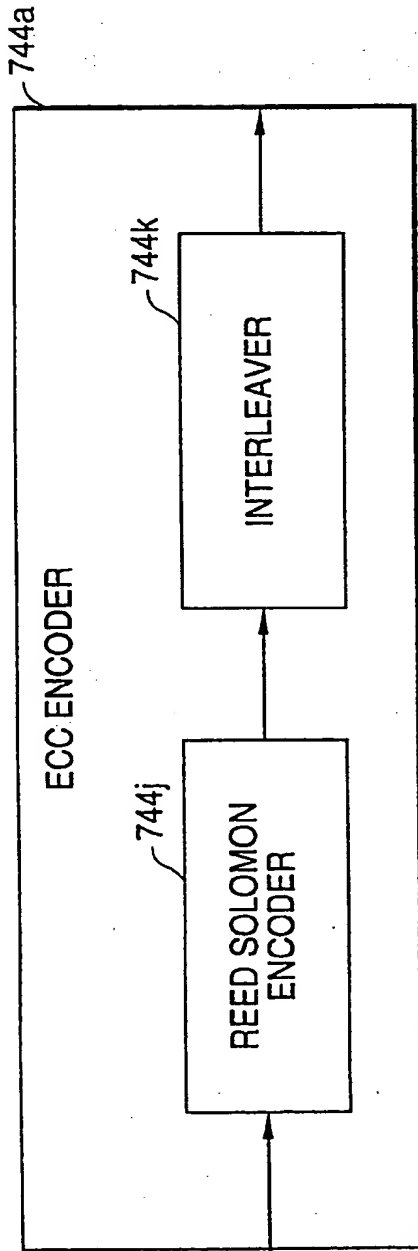


FIG. 160(a)

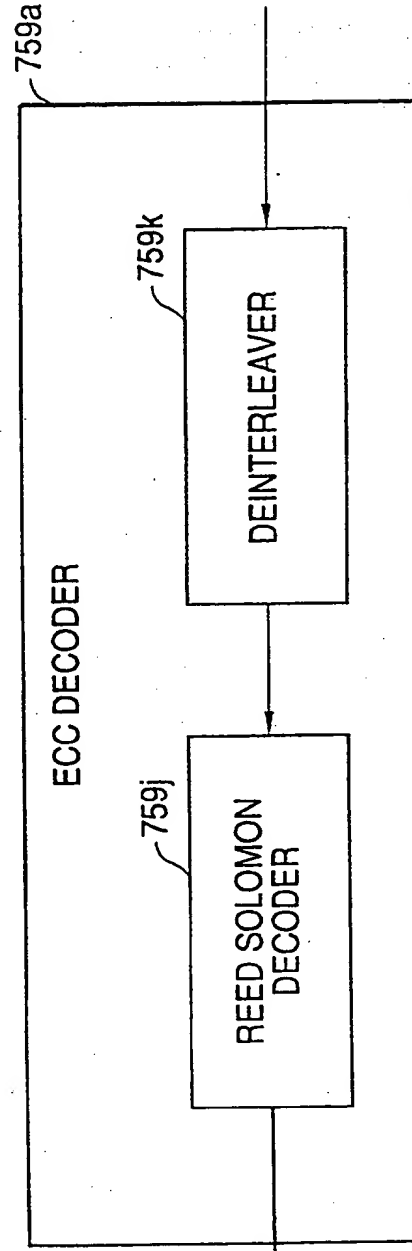


FIG. 160(b)

FIG. 161

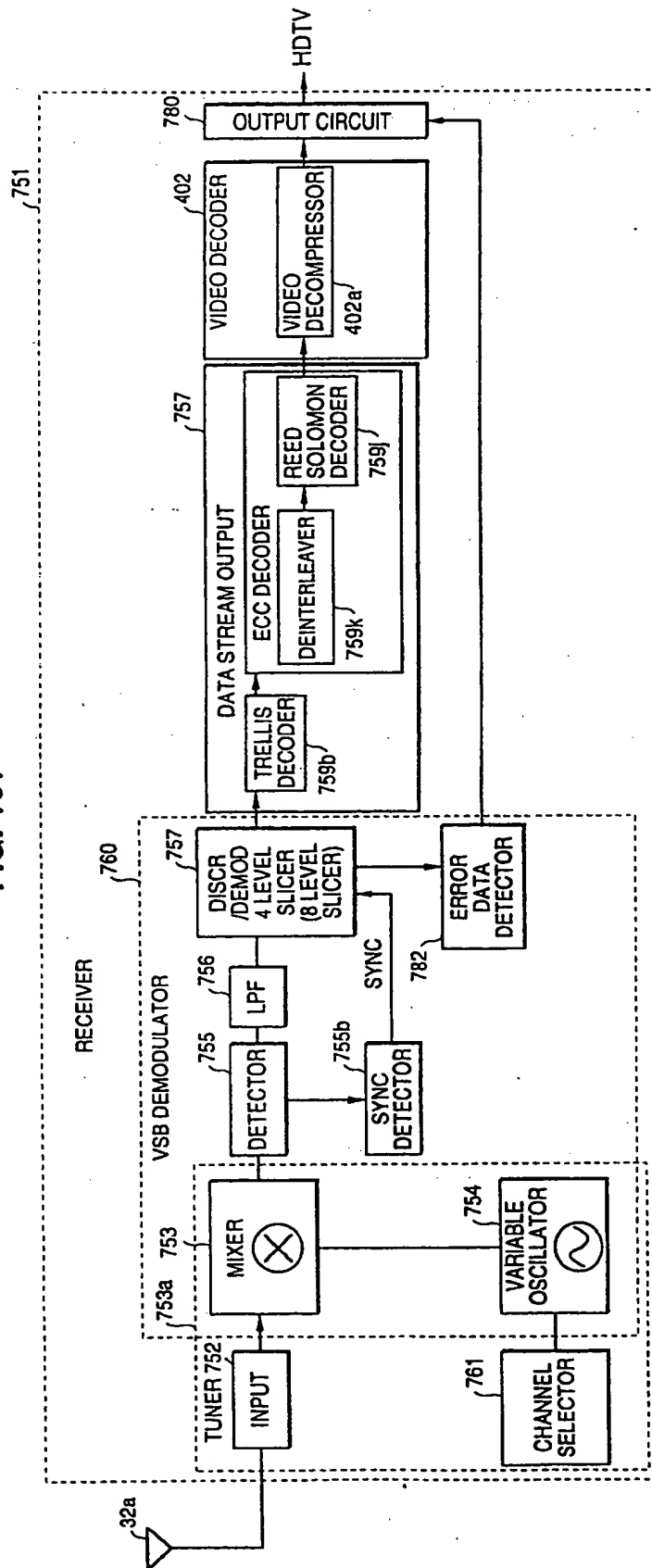


FIG. 162

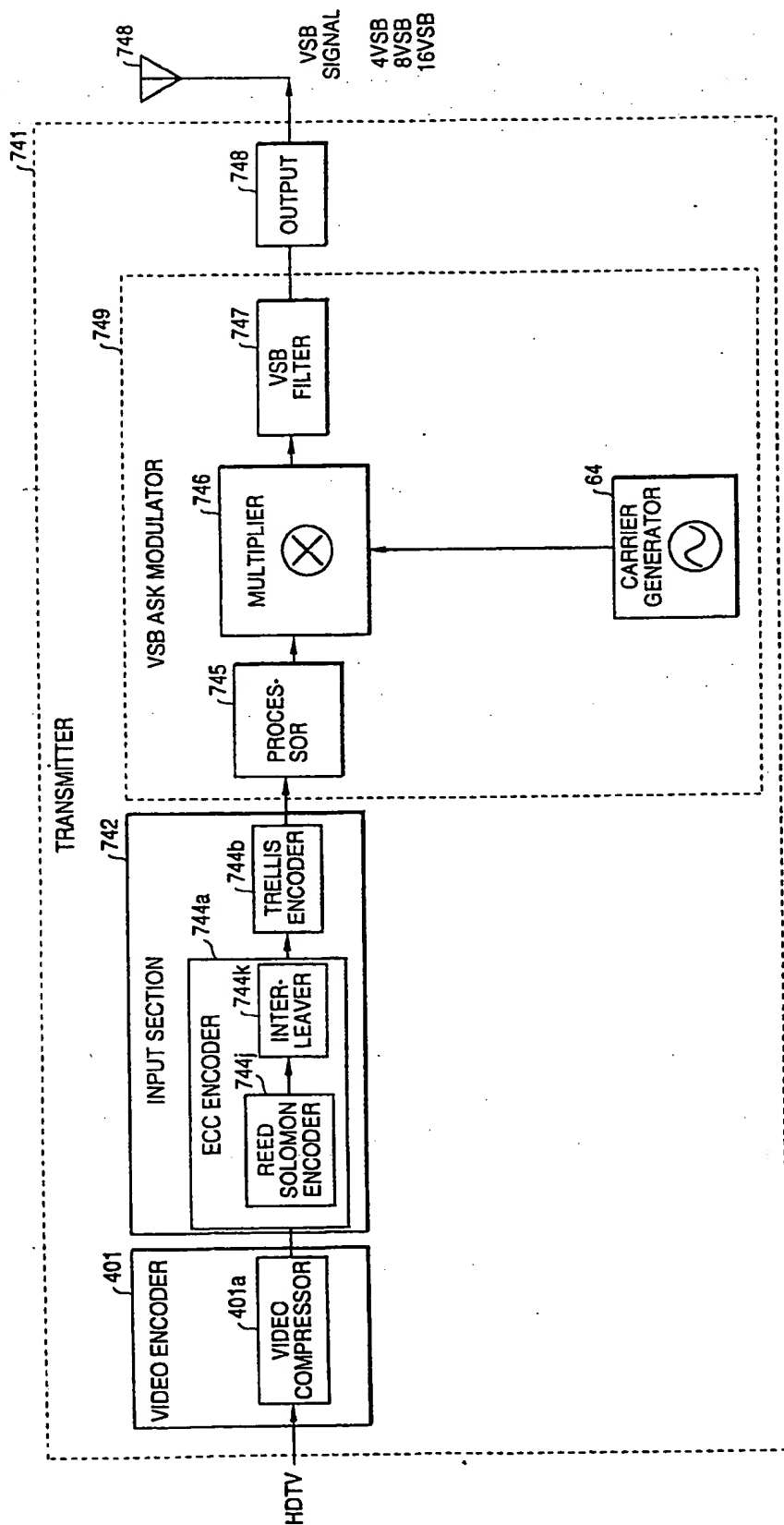


FIG. 163

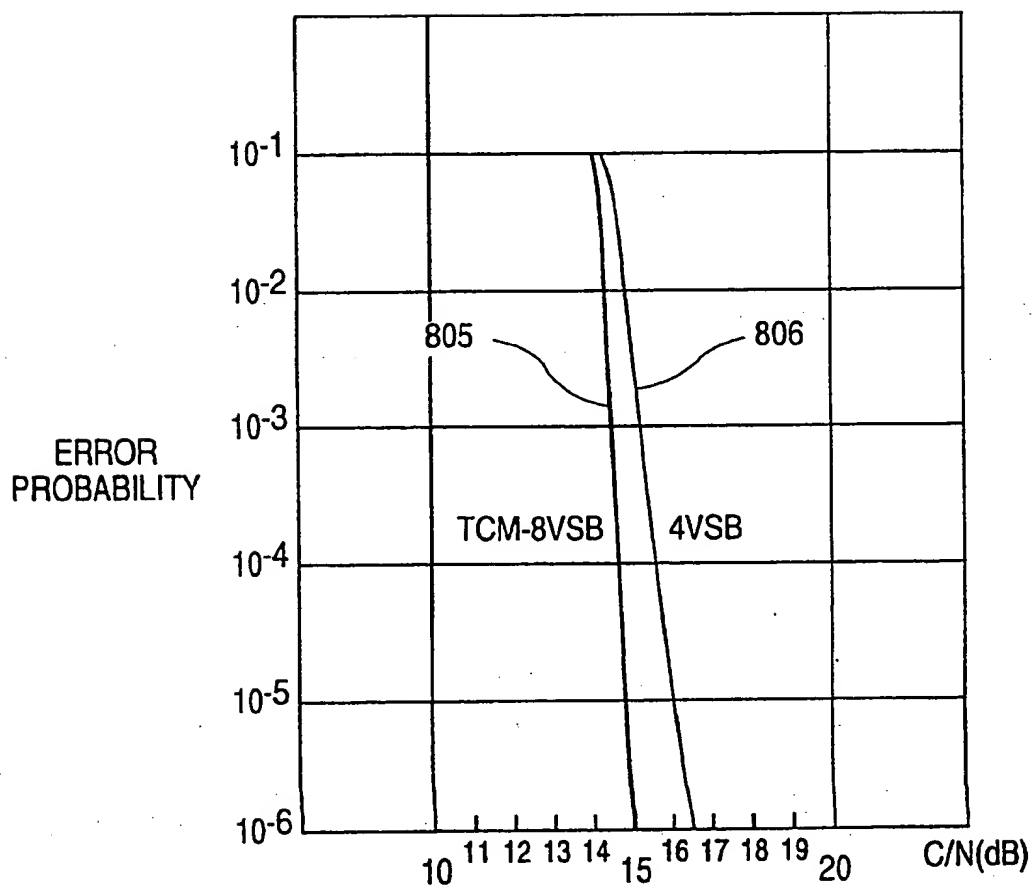


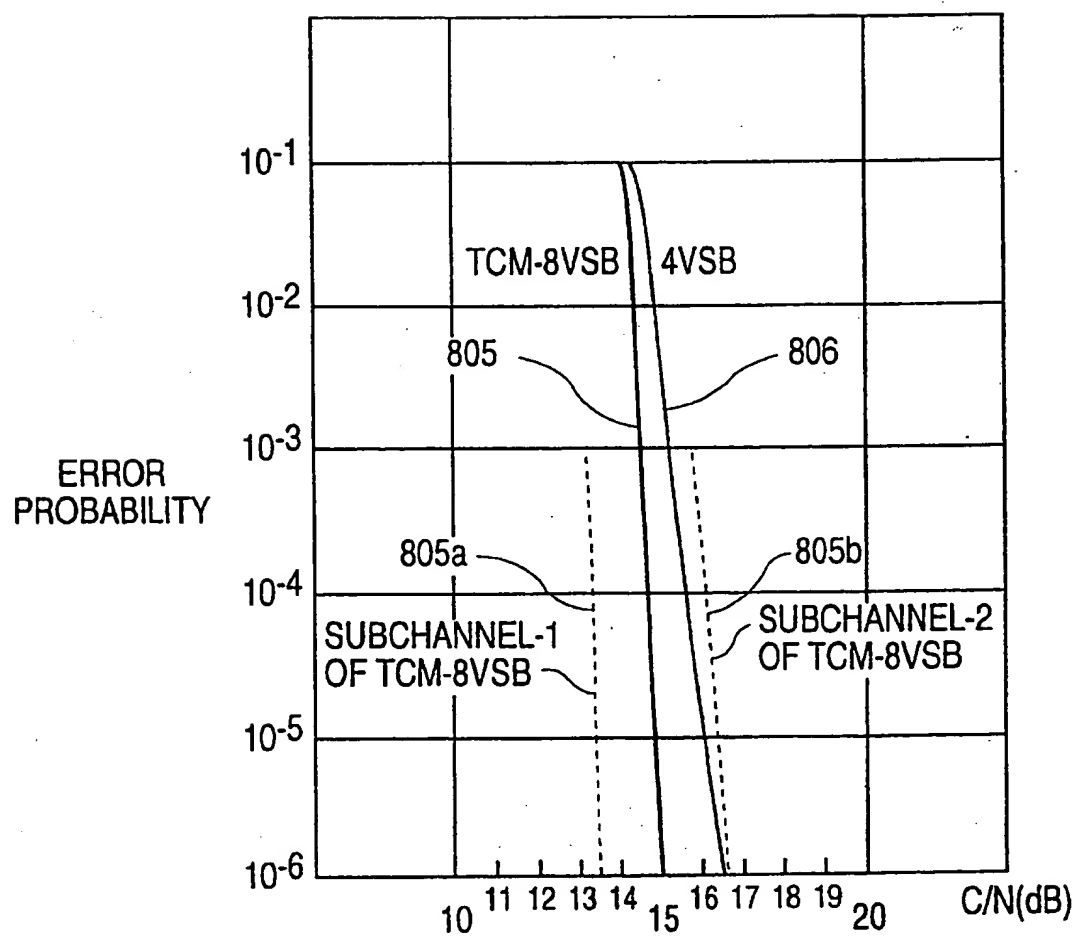
FIG. 164

FIG. 165(a)

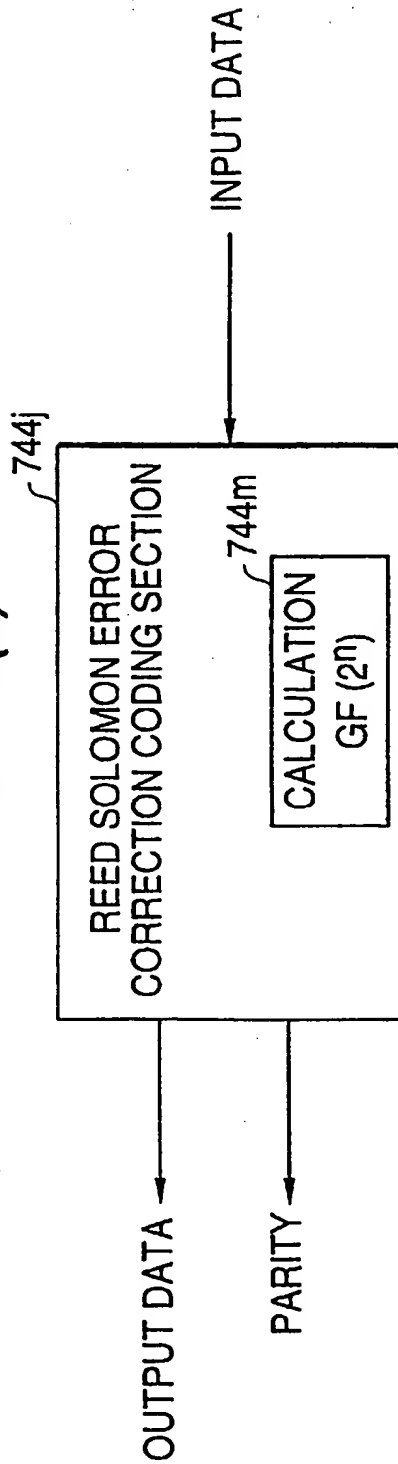


FIG. 165(b)

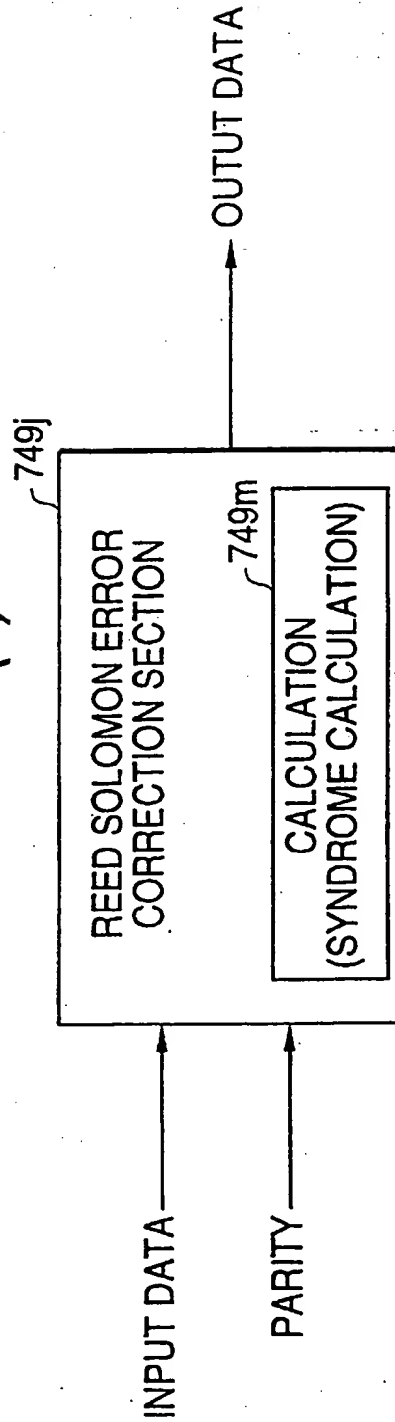


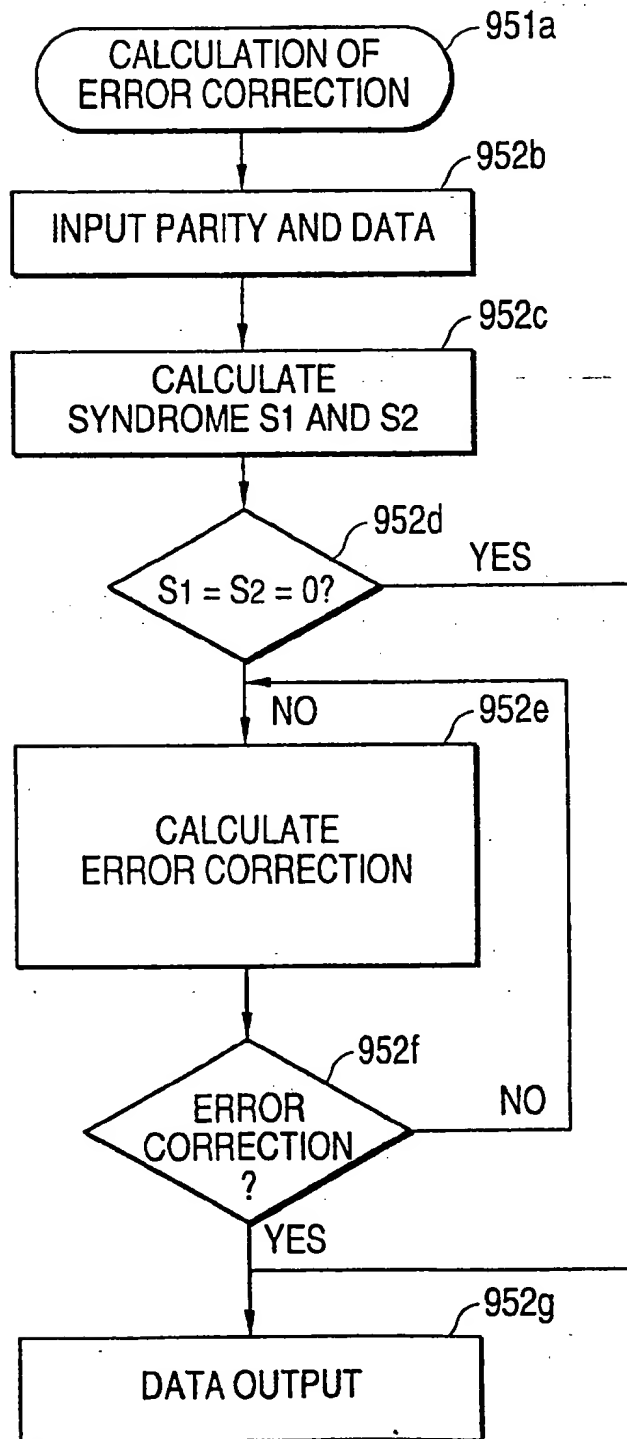
FIG. 166

FIG. 167

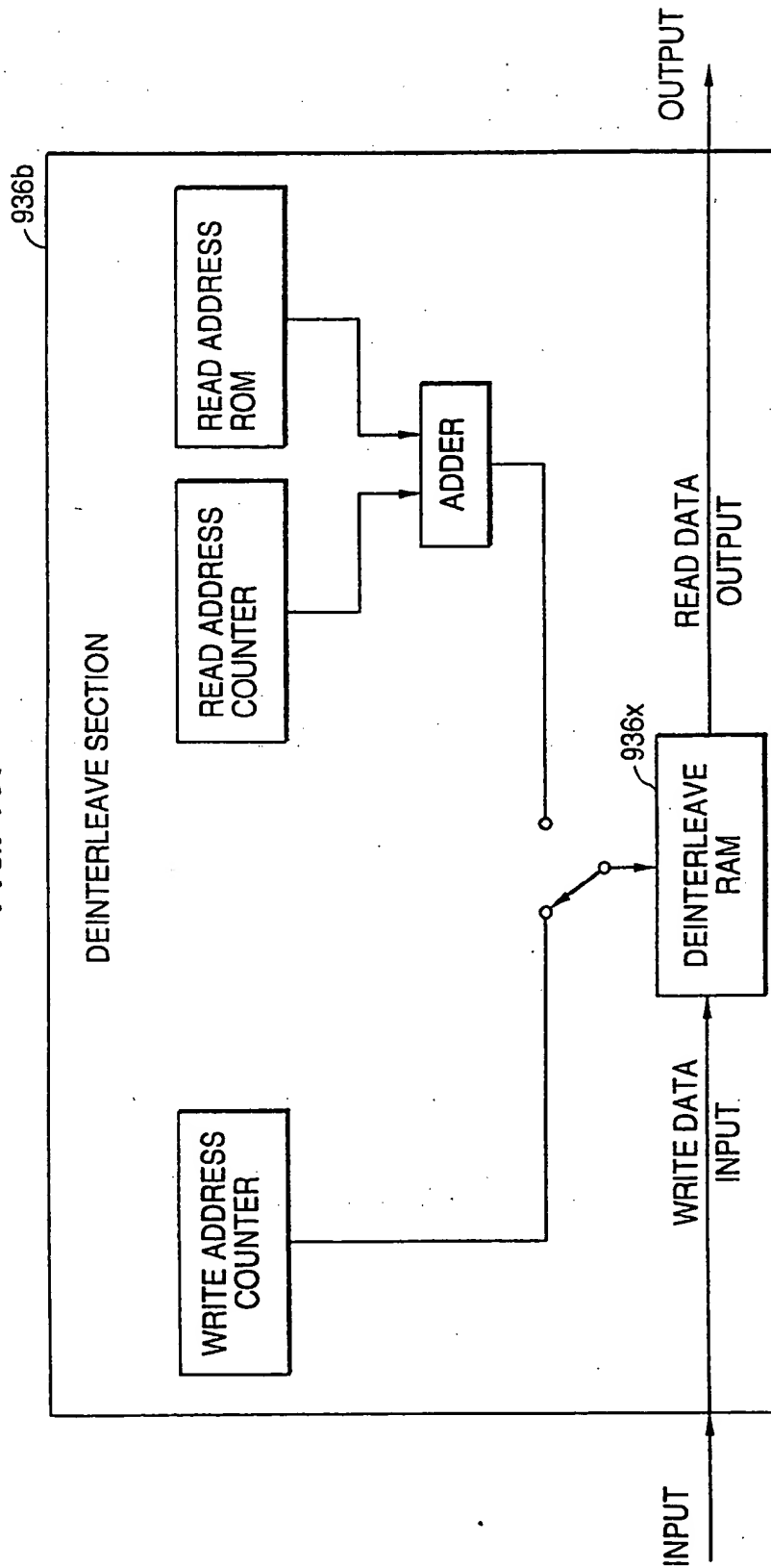


FIG. 168(a)

INTERLEAVE TABLE

1	2	3	4	5	6	7
DATA						C2 PARITY
1	A 1	A 2	A 3	A 4	A 5	A 6
2	B 1	B 2	B 3	B 4		
3	C 1					
4	D 1					
5	E 1					
6	F 1					
C1 PARITY	PARITY	PARITY	PARITY	PARITY	PARITY	PARITY

FIG. 168(b)

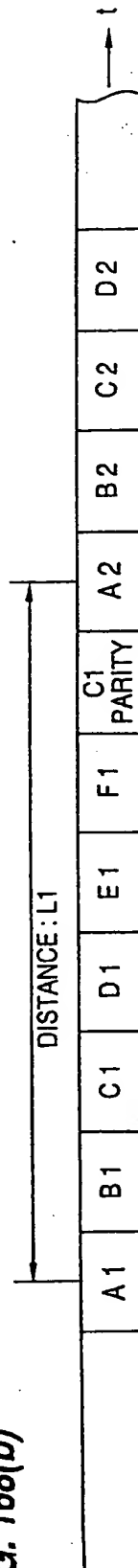


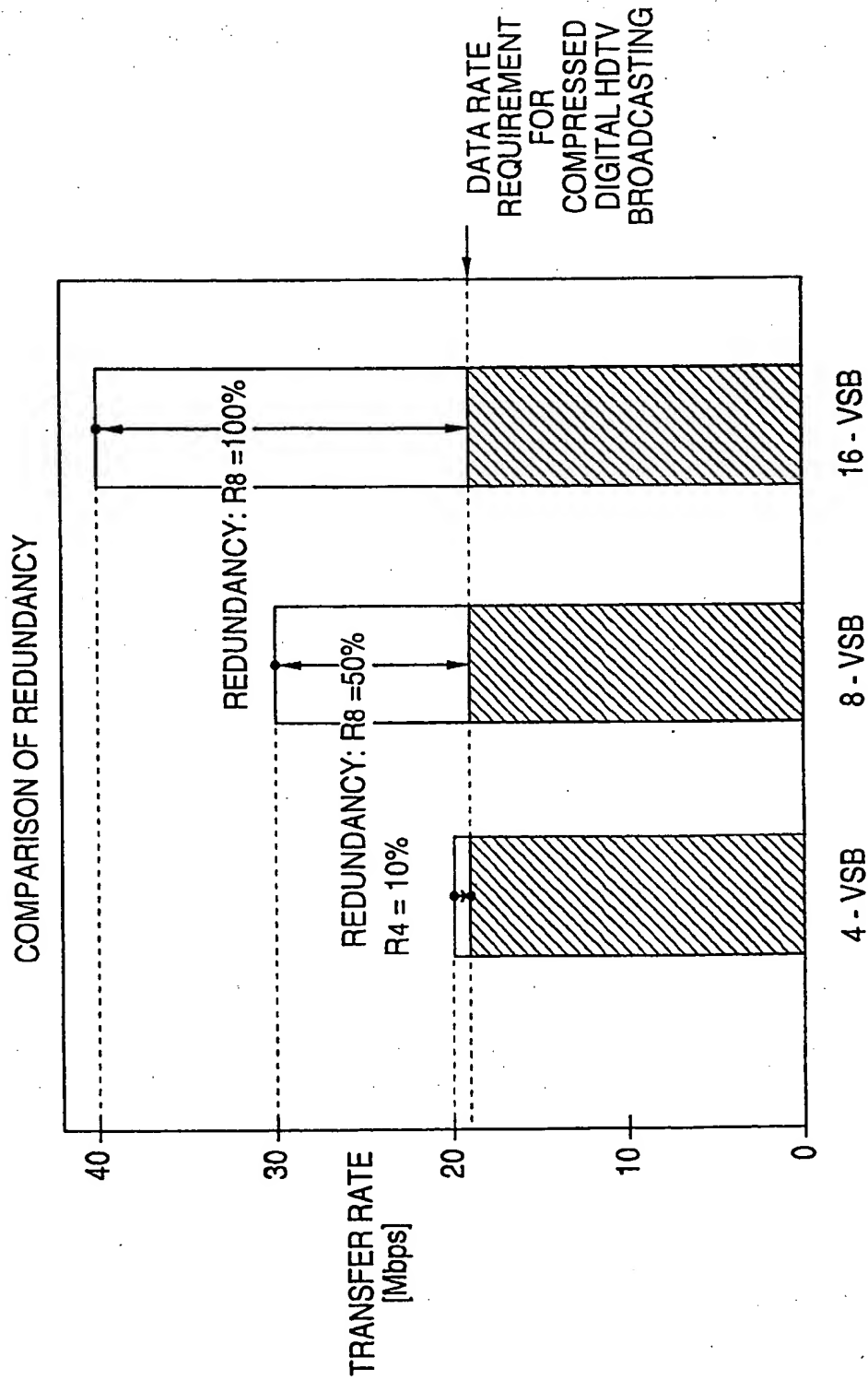
FIG. 169

FIG. 170

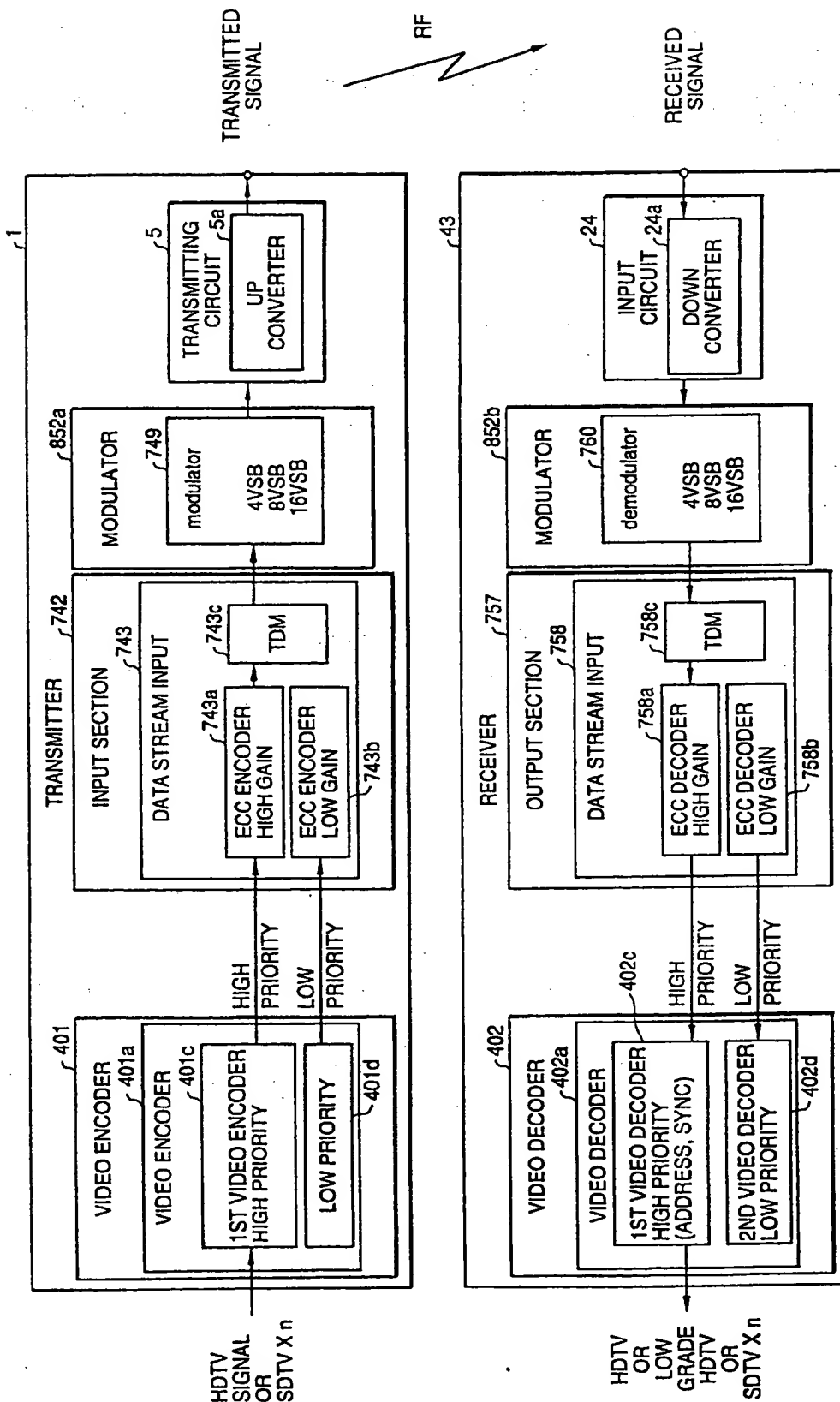


FIG. 171

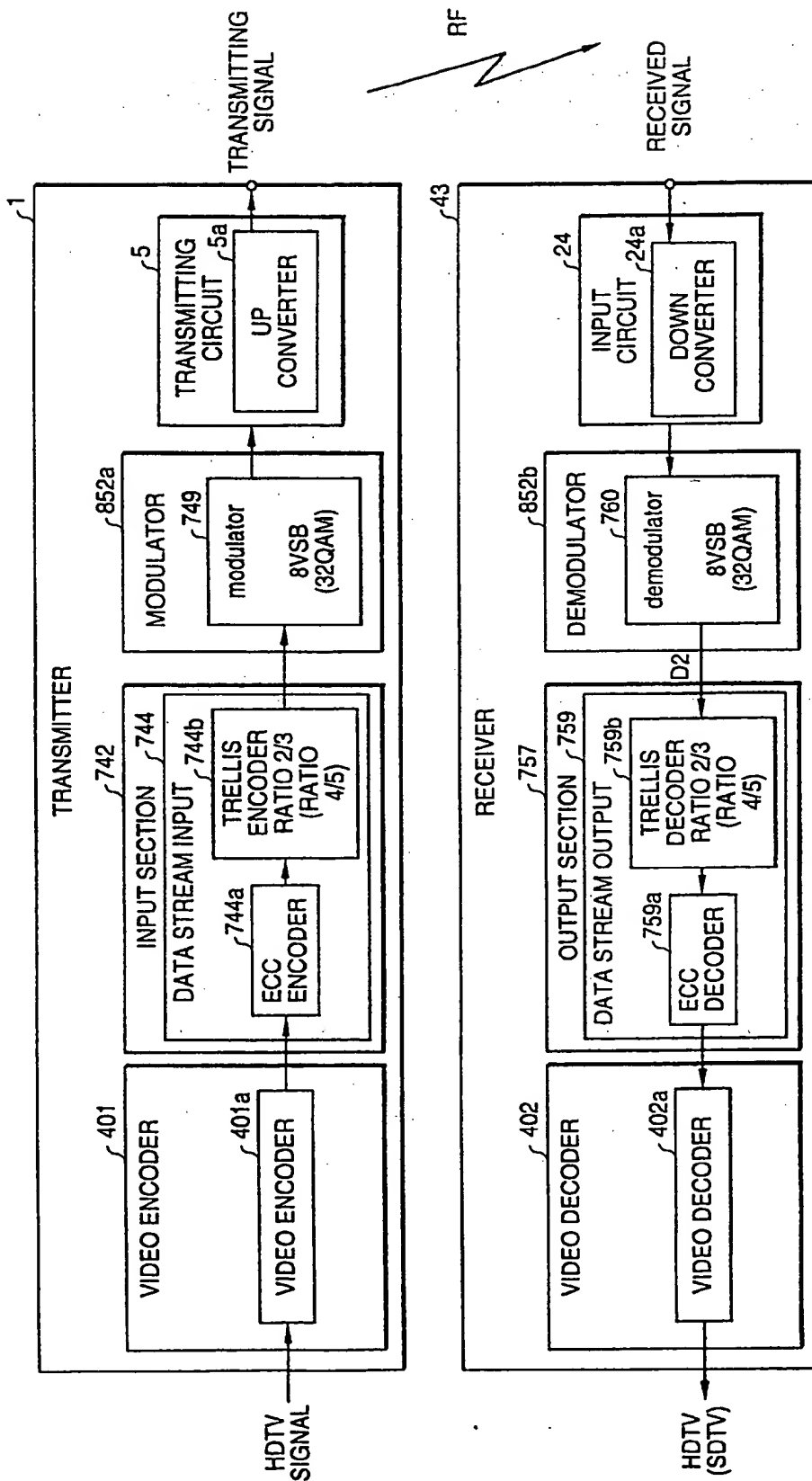


FIG. 172

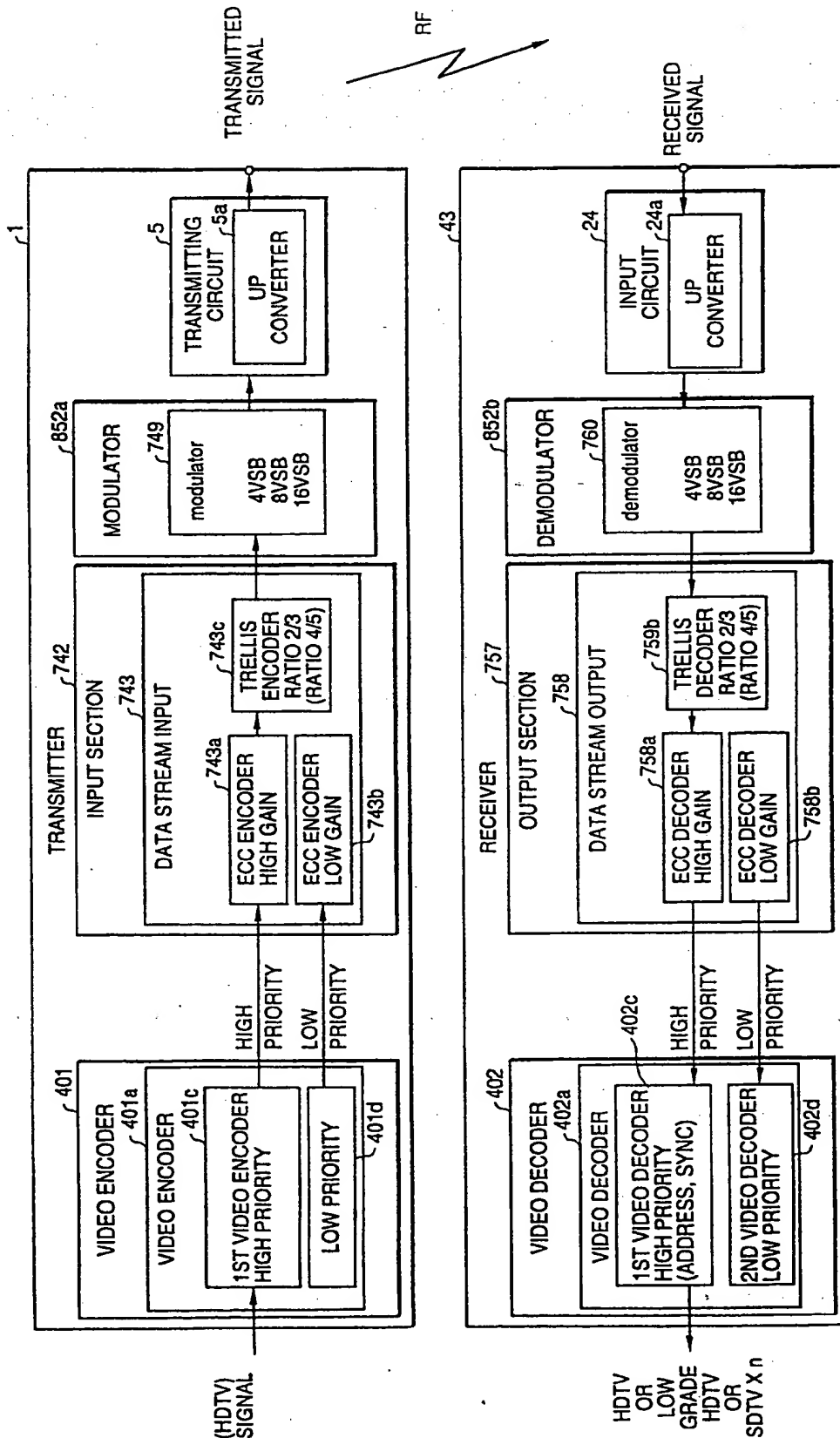


FIG. 173

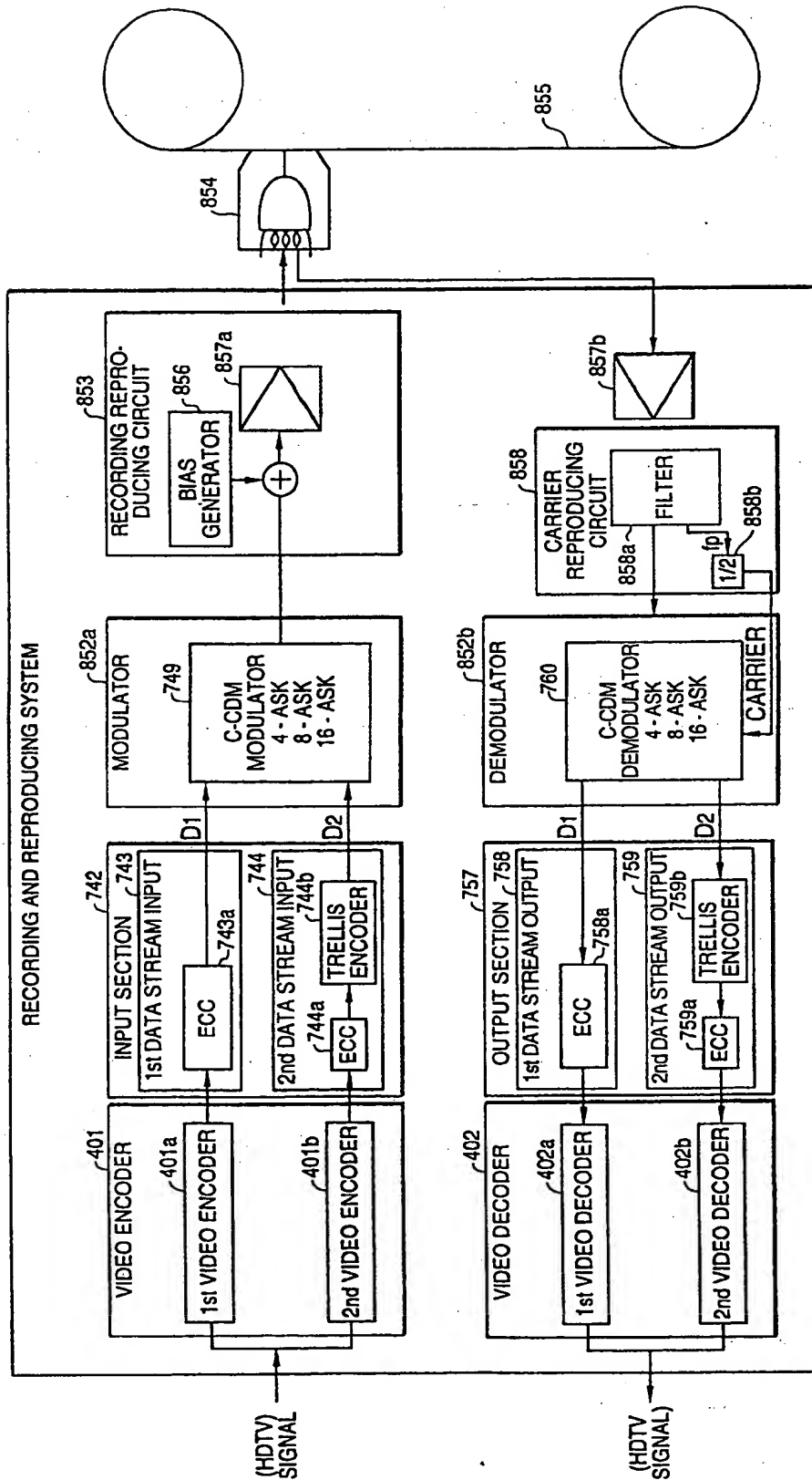


FIG. 174

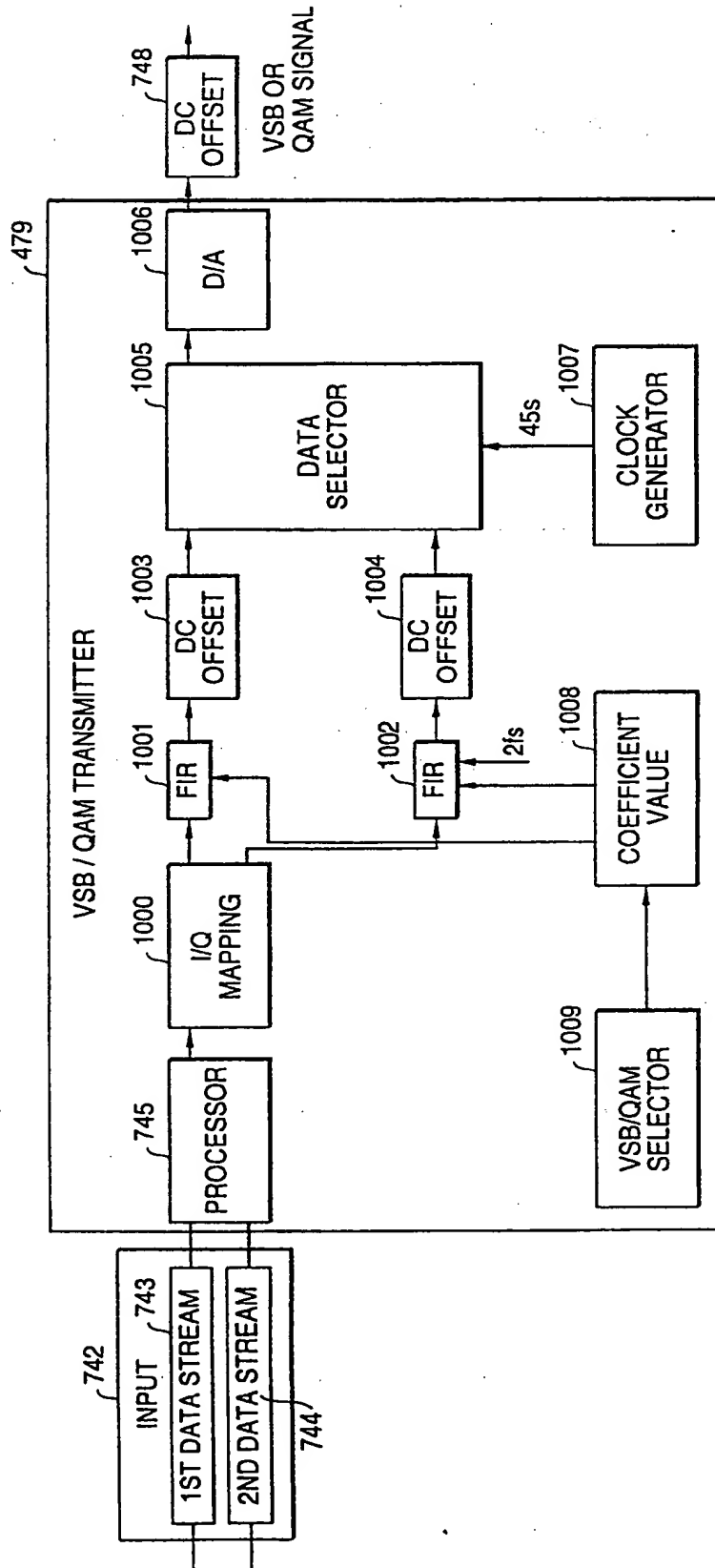


FIG. 175

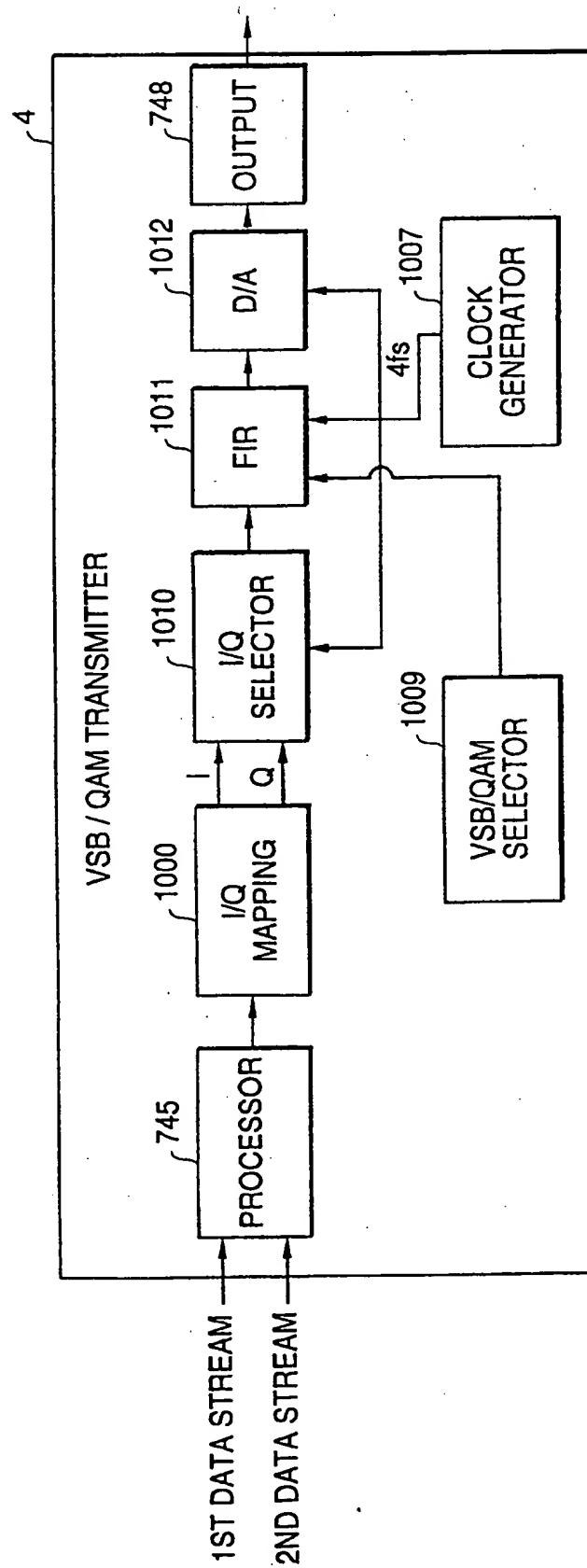


FIG. 176

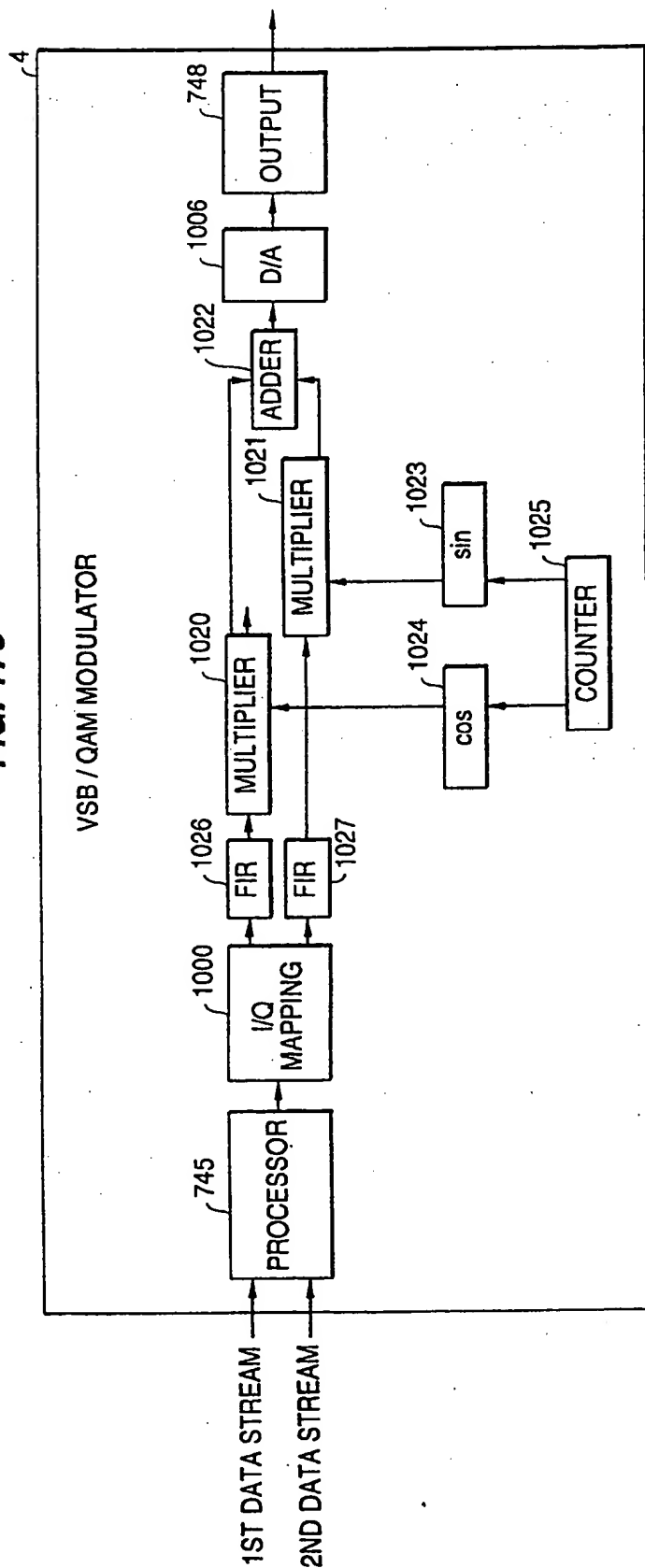


FIG. 177

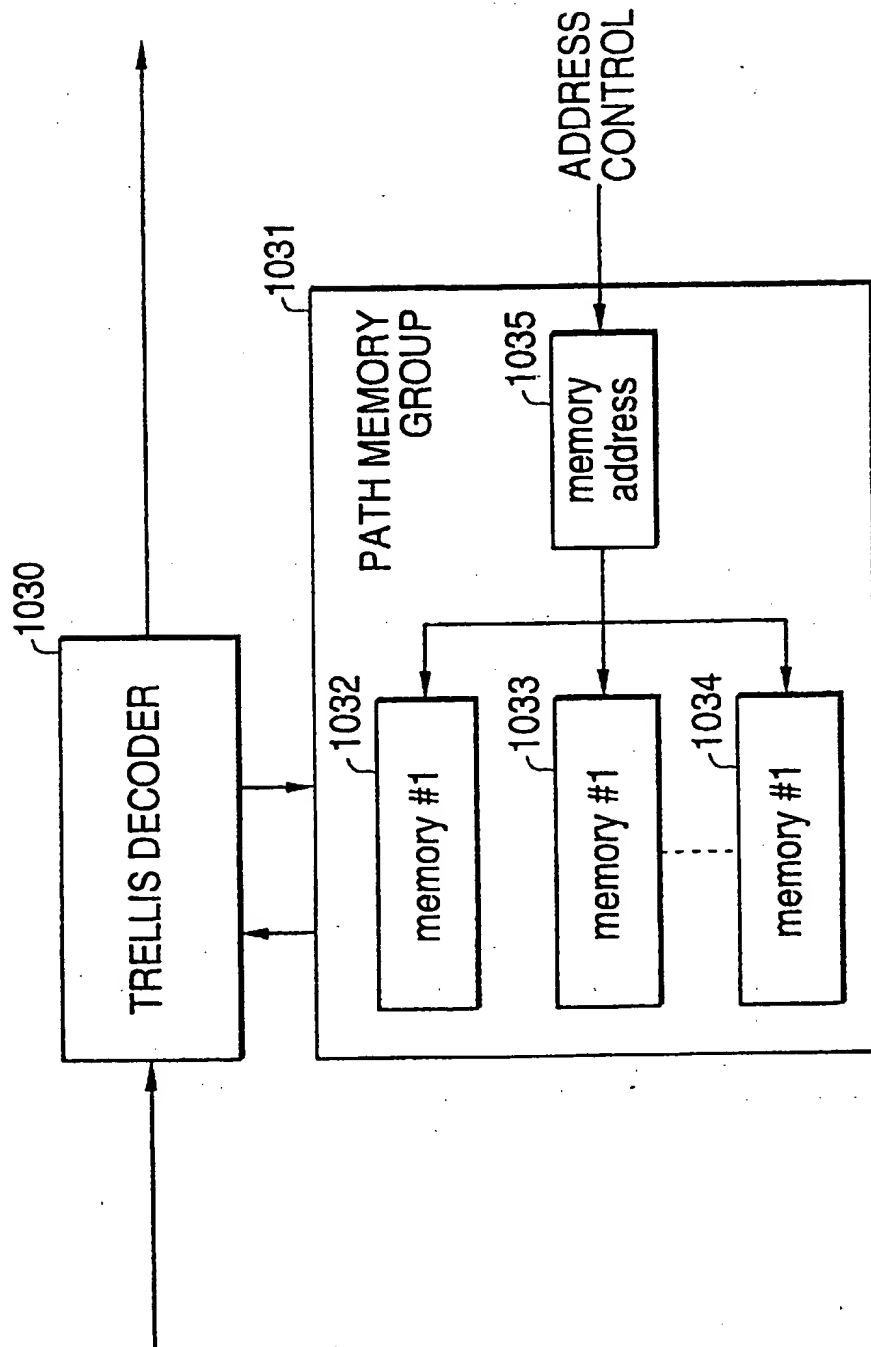


FIG. 178

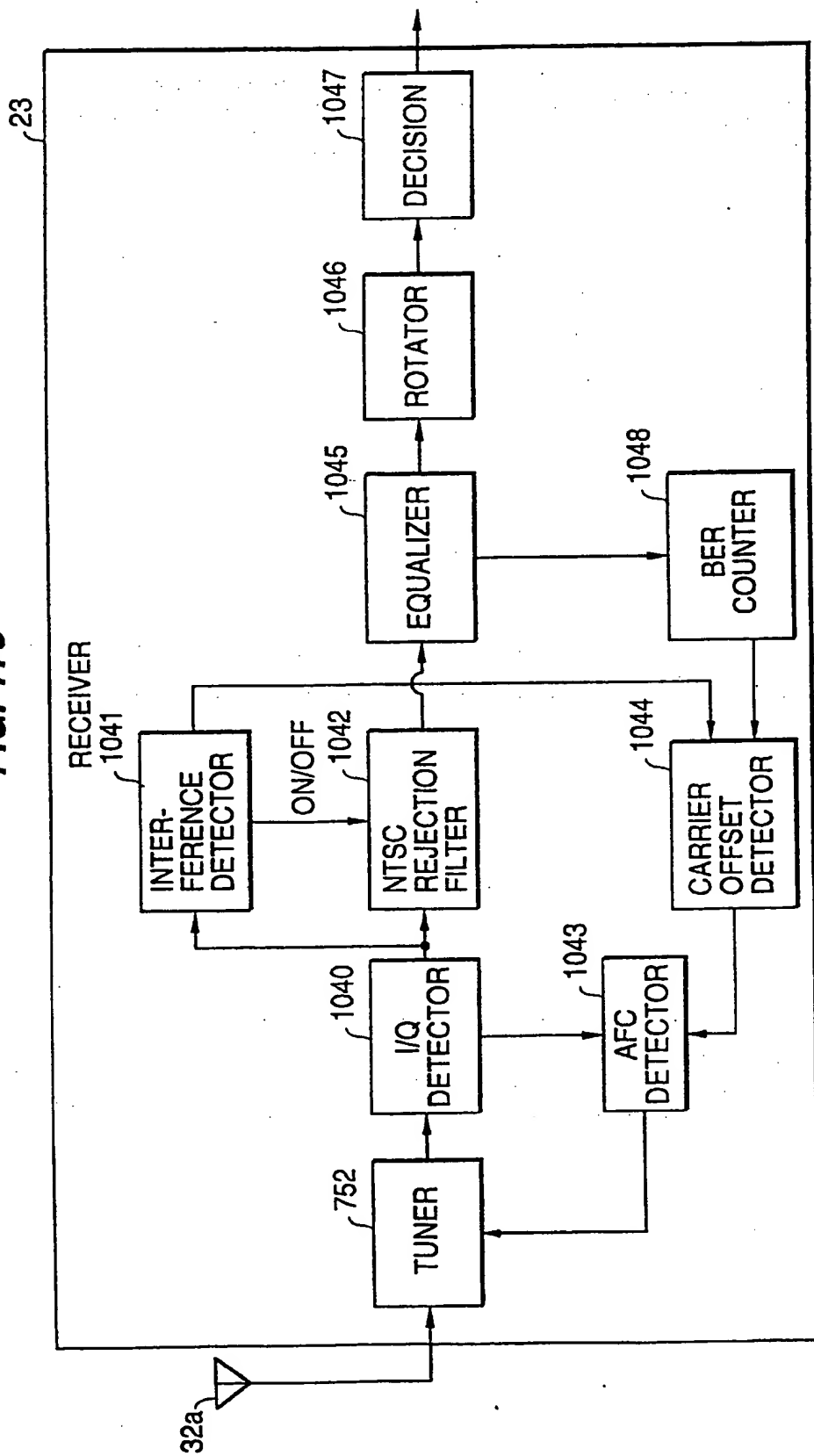


FIG. 179

